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Celadon Probes

A Guide to Contact Resistance, Frequently Asked Questions, and Best Practices

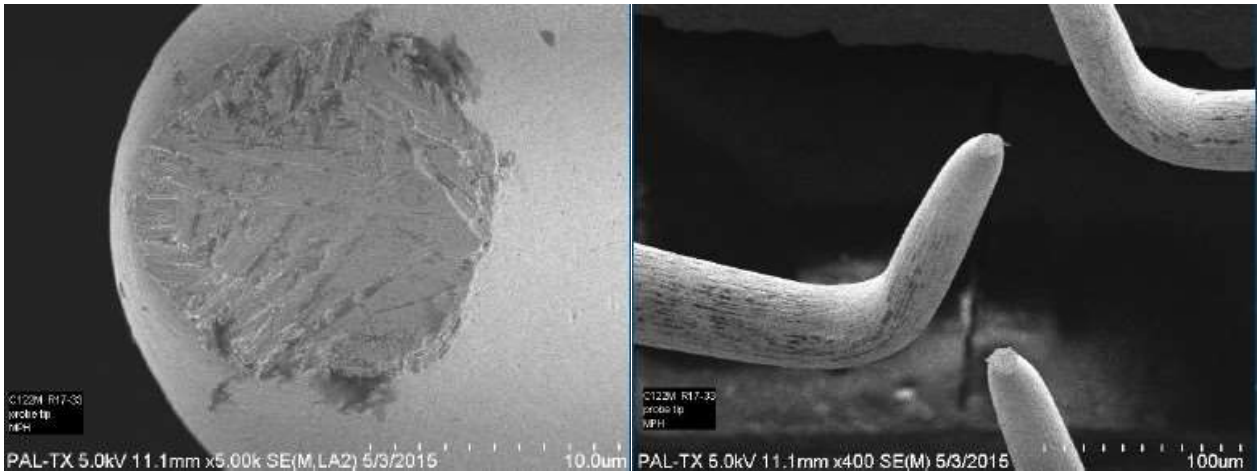

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TABLE OF CONTENTS

1 INTRODUCTION: WHAT IS CONTACT RESISTANCE, AND WHY DOES IT MATTER

This guide provides information on Contact Resistance [Cres] as measured in ohms [Ω] from probe tip to bond pad on semiconductor wafers. Cres is an electrical quantity that measures how the contact area between the probe and the pad impedes the electrical flow.

Why is this important? Low Cres helps preserve the electrical integrity of data collected. If Cres is not properly managed, it can cause offsets in data as well as increase the risk of melting probe tips.

Cres is also important to manage the lifetime of the probe tips on a probe card. In high current applications, if Cres rises due to embedded particles in the tip or oxidation, you are trying to push what previously was a manageable amount of power, through a smaller area. If Cres gets too high, the probe tip will be damaged, or melt completely, causing significant cost to repair the card.

Properly maintained probes will remain stable for test for a long time, but only if the correct cleaning recipe is used.

For the “Celadon Toothbrush” cleaning method, please follow the link below for off-line cleaning.

https://www.youtube.com/watch?v=6lQT6TCs144

2 Frequently Asked Questions

- What cleaning process should I use for my probe cards?
  - This is one of the hardest questions that can be presented to a probe card vendor, as the exact process will vary significantly from customer to customer as their tests, conditions, and wafer materials vary significantly. In short, Celadon Systems does have some reccomendations, but the exact cleaning recipe varies from customer to customer based on electrical test performed, lab environment, and wafer material.

- To keep Cres low, it will shorten the life of my probe card, right?
  - While the best way to manage Cres is a more aggressive cleaning substrate, when used properly in tandem with a less aggressive medium for standard cleaning, you can still obtain extreme probe life in Celadon probe cards.

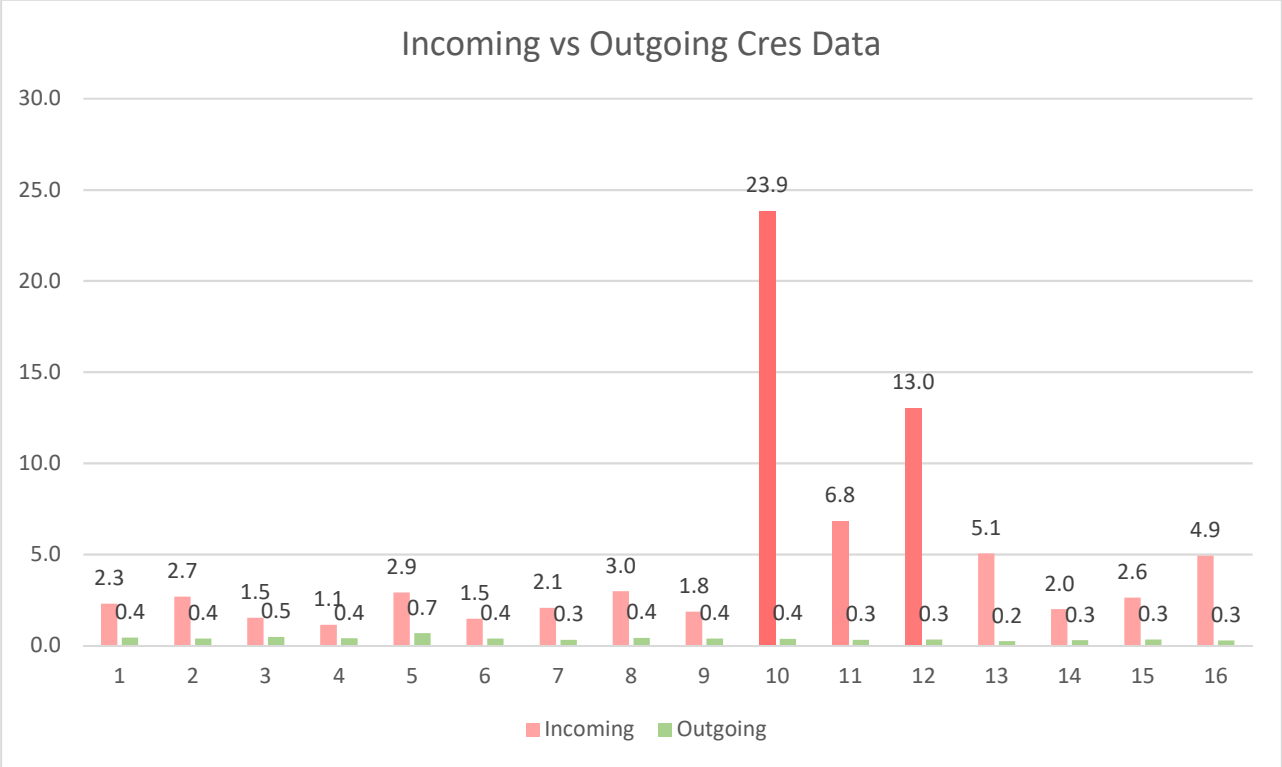
- Is In-Situ [In-Line] cleaning sufficient to maximize the life of my probe card?
  - While Celadon probe cards are very robust, the optimal regiment for a probe card is a balance of: In-Situ cleaning using prober auxilary chucks with cleaning substrates or cleaning wafers, off-line cleaning with Celadon toothbrush, and bi-annual Probe Maintenance [PM] at Celadon headquarters [details on PM service in section 3]. When properly maintained, Celadon probe cards are capable of reaching 10+ million touchdowns [ref:1].

3 Contact Resistance Management – Best Practices

The best way to keep your Cres low, is with proper probe maintenance. While the exact process and cleaning materials vary from customer to customer, Celadon reccomends the following steps to help dial in cleaning.

Problem: High Cres after testing multiple wafer lots [normally cres doesn't increase with a single test, it is a slowly increasing value as more and more particle are embedded in the tip of the probe, degrading the electrical signal and impending the current flow].

Below is actual test data taken from an incoming probe card with Cres issues in the field. Celadon took incoming Cres measurements on a blanket Al sputtered wafer.



After the card is received at Celadon the card goes through an alcohol and hot water bath, followed by clean air dry, then baked for 2-4 hrs. This bath/bake process of the PM cleans to manage leakage. The Cres management is accomplished by touching down the probe card on a Tungsten Carbide [WC] substrate or Celadon Tungsten Carbide Cleaning Wafer. For best results with Tungsten Carbide cleaning substrate **the overdrive used on the substrate should match that of your test environment.**

For In-Situ cleaning, we recommend ITS Probe Polish 99, the different part numbers are as follows for various systems.

TEL P8/P8E	PP-2001-9903SC/I-M, 2” 99% ITS
EG4085	PP-2010-9903SC/I-M, 1.5”x1.5 ITS
P8XL-LC	PP-2049-9903SC/I-M 4.25”
UF200	PP-2001-9903SC/I-M, 2” 99% ITS

Some production customers use probe polish as frequently as every 250-500 touchdowns/device contacts.

For ITS Probe Polish, touchdown up to 30 times in a step array, with at least 75 microns between steps. The stepping will prevent overuse of the gel pad that could result in picking up polish substrate particulate on the probes. Overdrive should be **over your normal test environment**, up to 100µm works well. The probe polish will also need to be changed on a regular basis.

When Cres gets too high, only then do you use a WC plate or wafer to remove embedded particles and oxidation.

4 EXISTING CLEANING RECIPES FROM THE FIELD

- FACTORY 1: Does no cleaning inline at all. When they see a CRES increase, they pull the card and send it to the probe card repair shop for an offline "toothbrush clean". This rarely happens. Some cards that have been in use for months and years and never cleaned at all. This factory sees extremely long probe card life, but they have no way to count TD, so we don't have any exact counts. They run older technology.

- FACTORY 2: Uses PP70. After 175 touchdowns, they clean. Cleaning recipe is 15 touches. OD into cleaning material is the same as on the wafer, 30um. (We optimized their scrub for 30um, FYI. Normally it would be 45-55um.) They have been running 24/7 on our cards since late 2016, and lifetimes are in excess of 5M.

- FACTORY3: Uses PP150. Every 60 touchdowns, they clean. Cleaning recipe is 10 touches. OD into cleaning material is 30um, and OD into wafer is 70um. (Our opinion is this recipe is possibly too aggressive, so if they are not happy with card lifetime, we will work with them to make this recipe more moderate)

- LABS: They tend to use aggressive cleaning media. One engineer likes Tungsten Carbide for WLR testing. She doesn't care too much about lifetime. She has long test times at elevated temperatures, so she is happy to sacrifice lifetime for low CRES because she will never need millions of touchdowns. All labs tend to be similar since lifetime is not a concern for them.

- NXP: Use PP99. OD into PP is 100um, and OD on wafer is 55um. They clean after every 250 TDs, touching probe polish 30 (2x15 pattern) times, then touch prober brush on occasion. Every 100K TD, they do a cloverleaf pattern on a tungsten block.

5 REFERENCES

Ref 1: Production Parametric Test – Challenges and Surprising Outcomes Running in a High-Volume Manufacturing Environment [produced in partnership with NXP {formerly Freescale} and presented at SWTW 2015]

6 CONTACT INFORMATION

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7 REVISION HISTORY

Revision	Changes	Date	Approval
1.0	Initial Release	6/27/17	GET
1.1	Updated to include UF200	7/25/17	GET
1.2	Recipes Added		