Customized probe card for on-wafer testing of AlGaN/GaN power transistors

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Outline

Introduction

- GaN for power switching applications

DC Characterization of GaN power devices

- CELADON probe cards
- Setup
- Measurements

Trapping effects in GaN HEMT

- Pulsed I-V
- Setup
- Measurements

Conclusions

Power switching applications

Power switching applications are a common presence in our daily-life.
Circuit designers and device manufacturers are constantly challenged to improve the present technology, in particular to achieve:

- Higher efficiency
- Smaller dimensions
- Lower costs

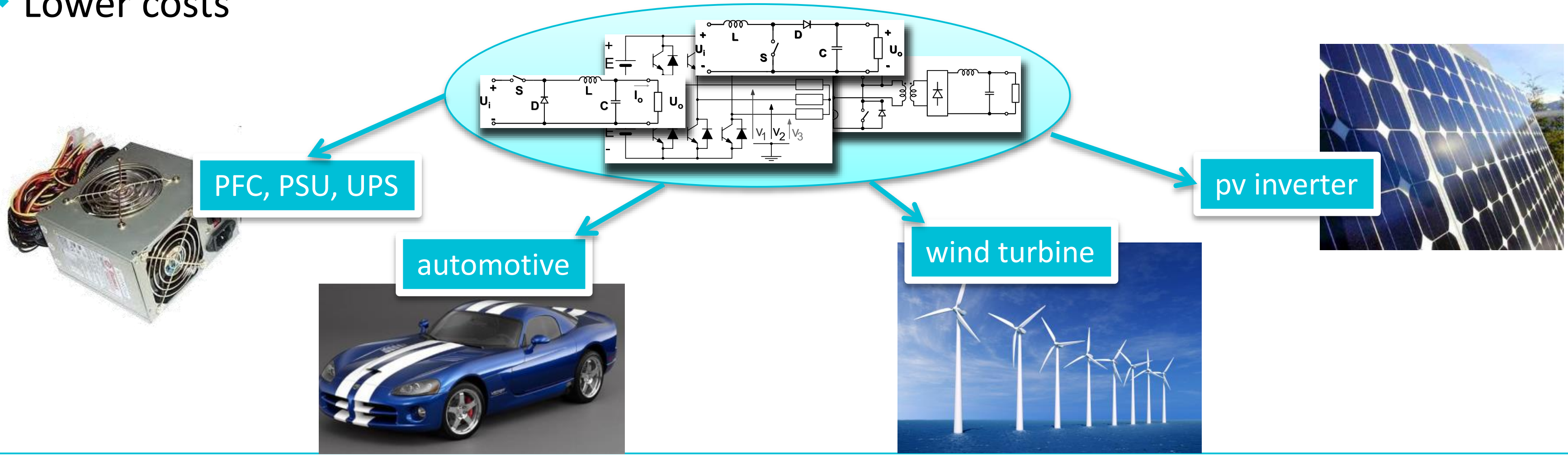
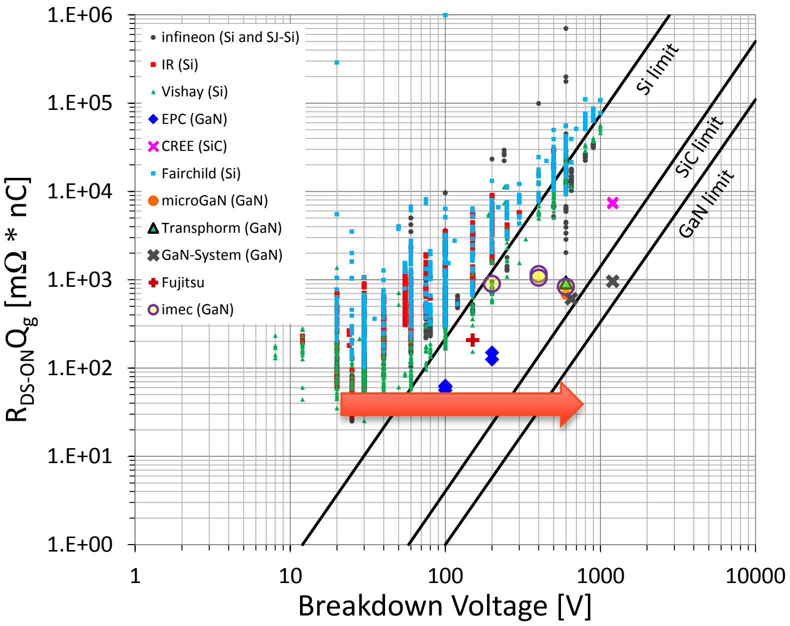


Figure of Merit

Devices with better $R_{DS\text{-}ON}Q_g$ and higher breakdown are needed to improve the circuit performance.



Silicon has reached its theoretical physical limits.

New technologies, such as GaN and SiC, will soon replace Si-based devices in power switching circuit.

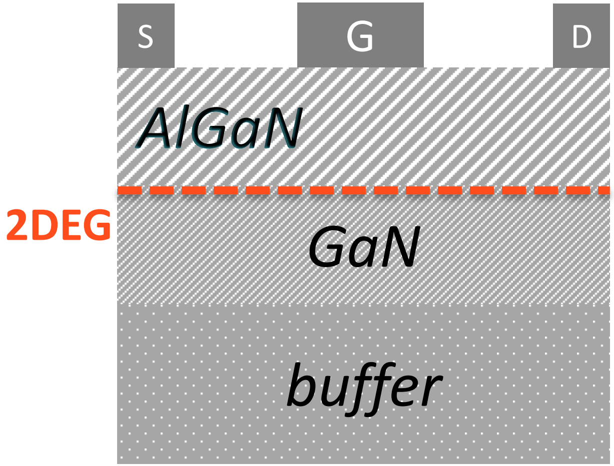
GaN-based devices

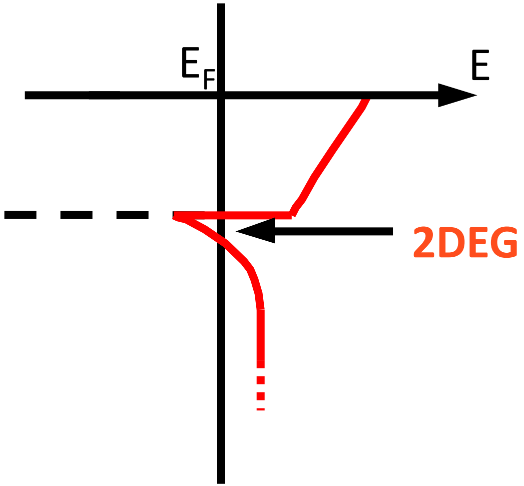
AlGaN/GaN High Electron Mobility Transistors (HEMTs) are attractive for power-switching applications due to their excellent properties:

- wide energy band-gap (high breakdown)
- high electron mobility (fast switching speed)
- good heat conductivity
- high density electron gas **2DEG** (10^{13} cm^{-2})

Property	Units	Si	GaAs	4-SiC	GaN
Bandgap	eV	1.1	1.42	3.26	3.39
Relative dielectric constant	-	11.8	13.1	10	9
Electron mobility	cm^2/Vs	1350	8500	700	1200-2000
Breakdown field	10^6 V/cm	0.3	0.4	3	3.3
Saturation electron velocity	-	1	1	2	2.5
Thermal conductivity	K	1.5	0.43	3-3-4.5	1.3

Depletion mode





Intrinsic normally-on operation (depletion-mode):

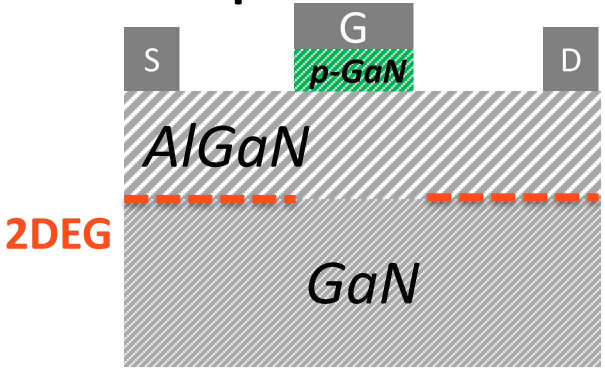
- Polarization-induced 2DEG

Normally-off operation (enhanced-mode):

- Fail-safe
- simpler gate control circuit

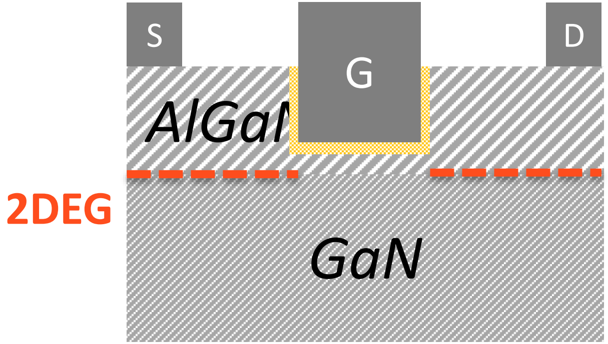
From d-mode to e-mode

p-GaN J-FET



A p-GaN layer below the gate lifts-up the band diagram below the gate to realize e-mode operation.

Recessed MISFET

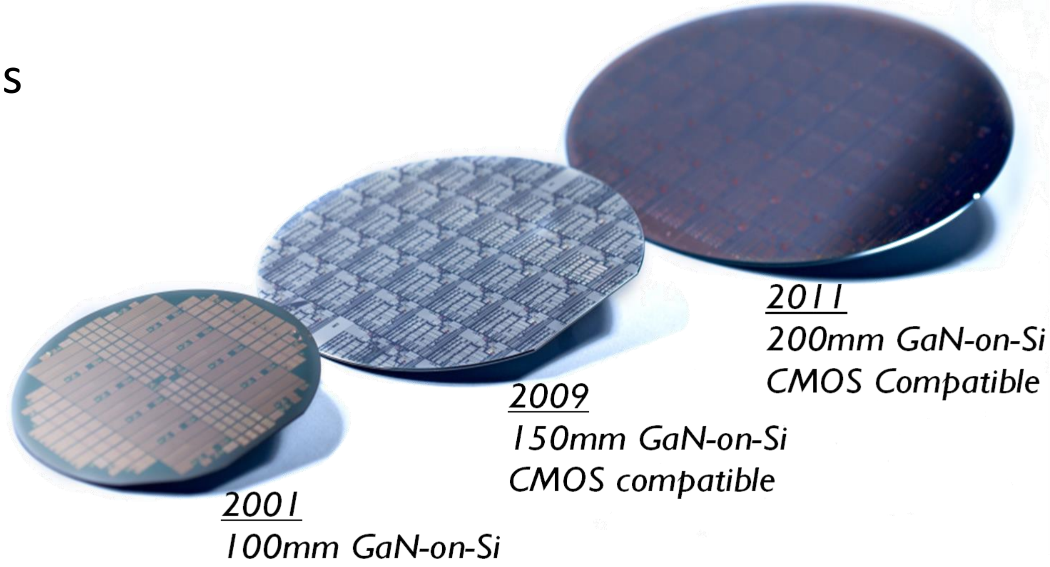


The AlGaN layer is recessed below the gate, to locally interrupt the 2DEG to realize e-mode operation.

Imec's R&D program on GaN devices-on-Si is meant to develop a GaN-on-Si process and bring GaN technology towards industrialization.

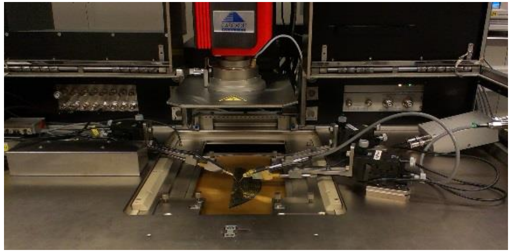
Imec R&D program highlights:

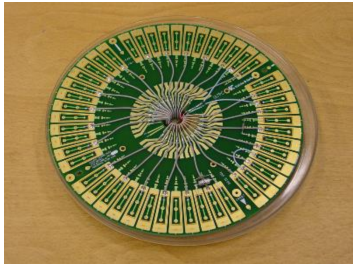
- High current, high V_{BD} devices
- E-mode operation
- 200mm (8 inch) epi-wafers
- CMOS compatible process
- Diodes co-integration
- Gold free ohmic contacts
- Advanced substrates



A new challenge for characterization

High switching speed, high power and the electrical behavior of the AlGaN/GaN power transistors call for specific characterization techniques in the power domain.



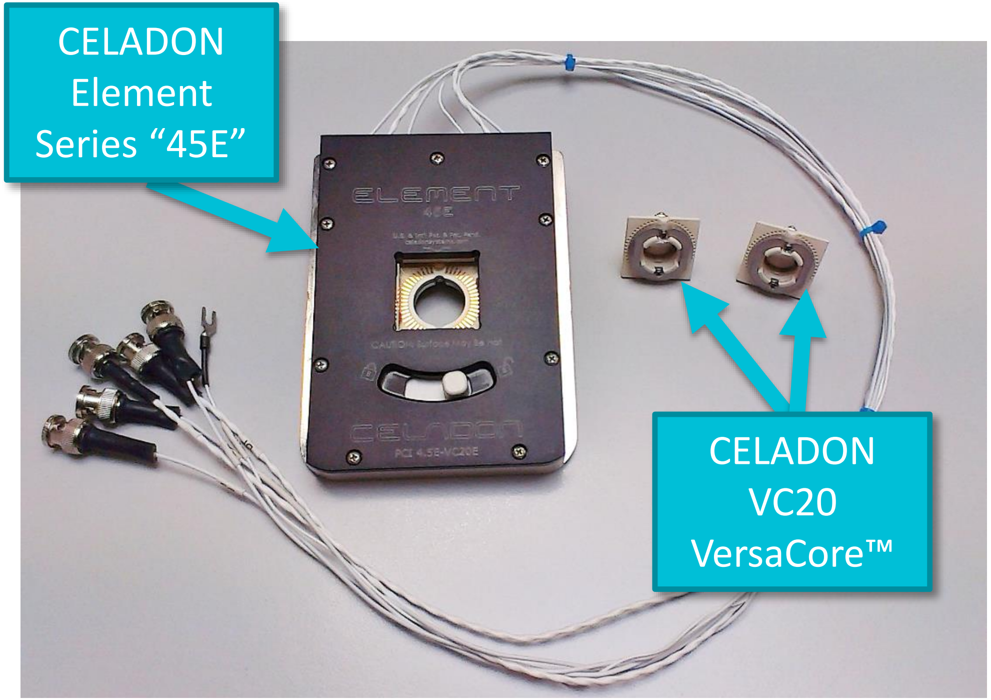


"Traditional" approaches:

- Limited current (for DC needles)
- Poor signal integrity required (for μs pulses)
- Low reliability at high temperature
- Short life time

New techniques are necessary for on-wafer power transistor characterization!

Customized probe cards



Our solution employs a CELADON VC20 VersaCore™ with multiple needles mounted on a 45E probe card adaptor.

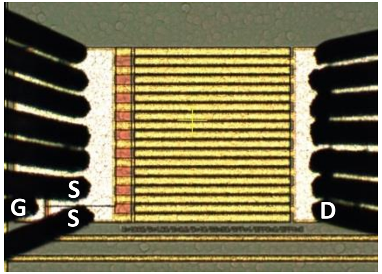
- High current measurements
- Low leakage (for breakdown measurements) less than 5fA’s
- Easy to swap between different probe card cores using Celadon’s insertion tool
- High temperatures (ceramic core) up to 200C

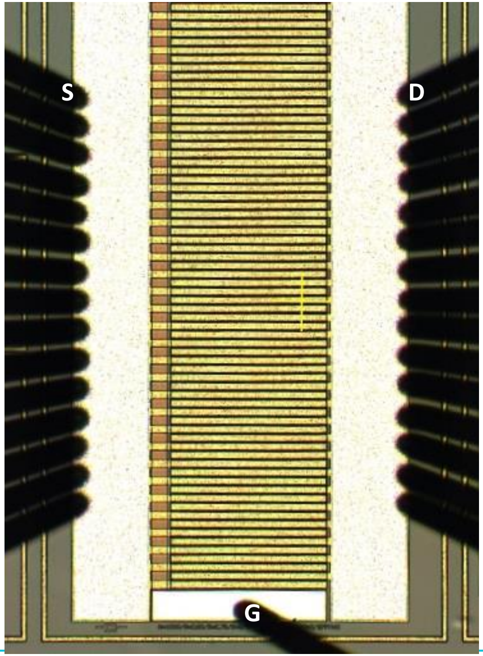
Different cores for different layouts

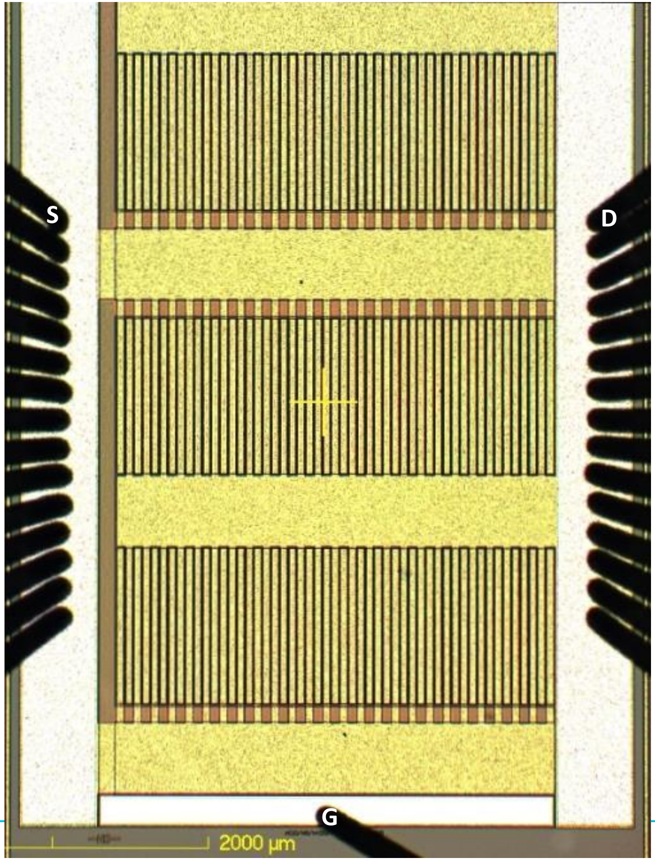
The cores are designed to satisfy the device specifications (layout, position of bond-pads, maximum current expected).

The large number of needles guarantees:

↓ lower contact resistance
↓ lower inductance
↑ higher maximum current

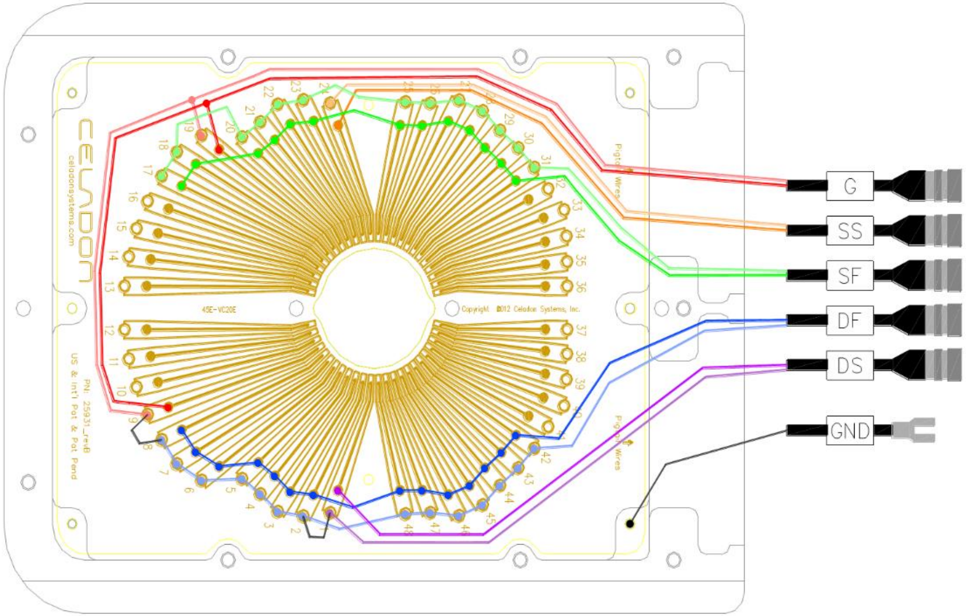






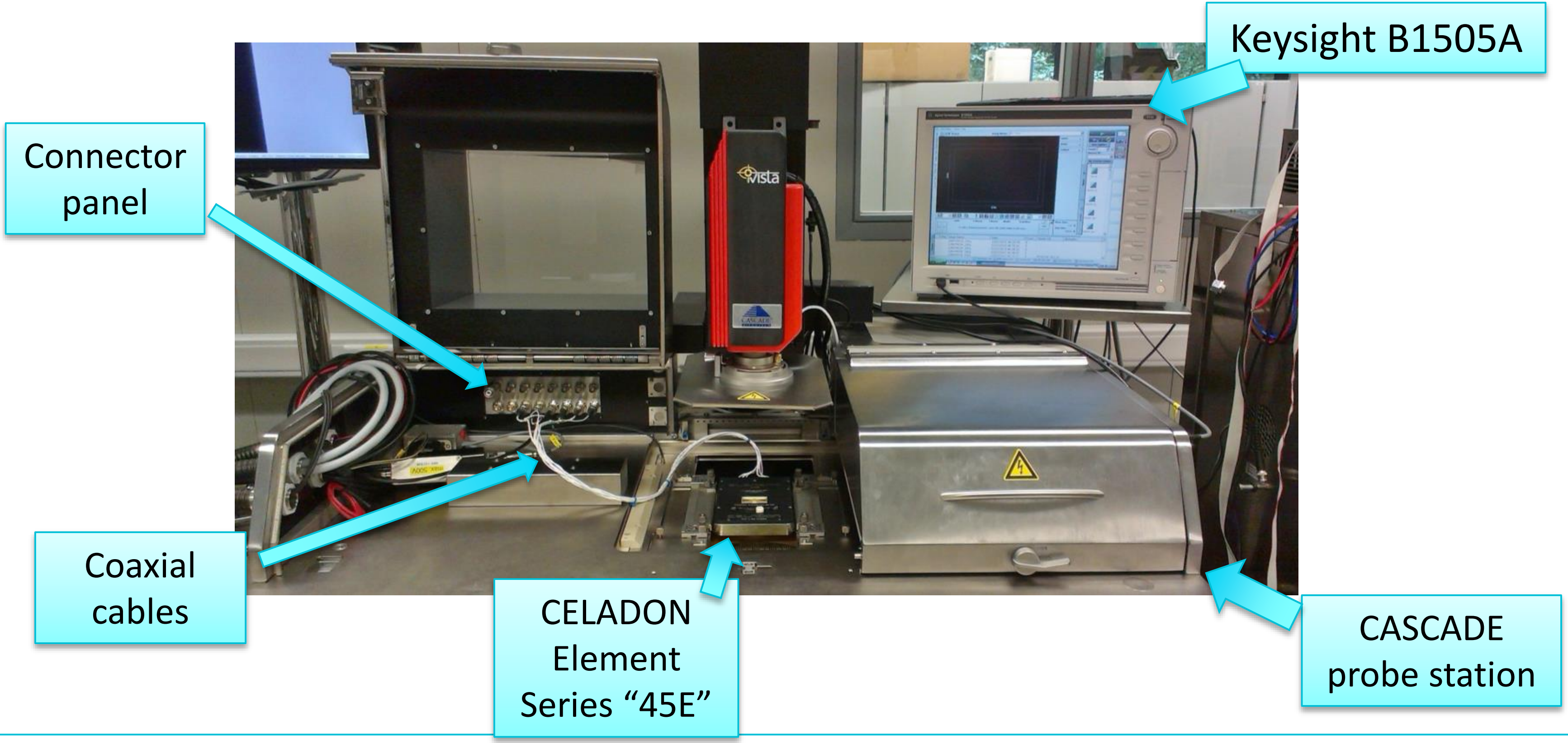
COMPASS
The Cascade Microtech users' community

Internal wiring



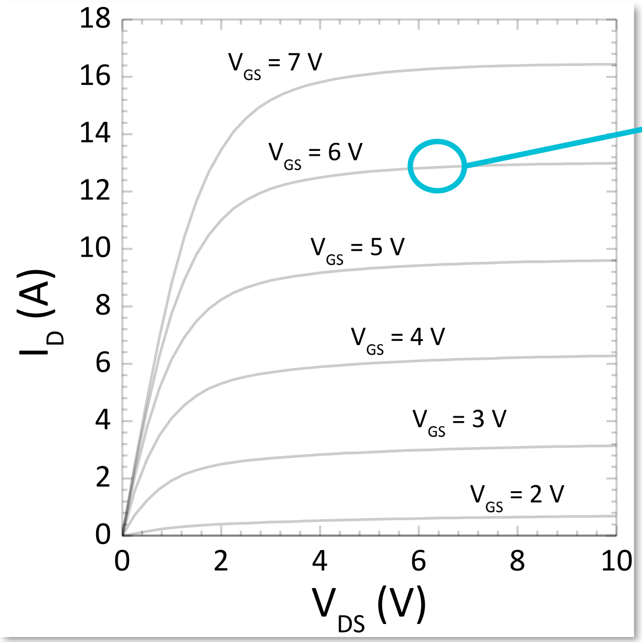
- Coaxial cables are used to contact the instrumentations
- Signal integrity is guaranteed by bringing the cable shield as close as possible to the needles
- Two isolated needles are reserved for the SENSE connections of drain and source
- Input (drain) and output (source) of the current are on distinct cables.

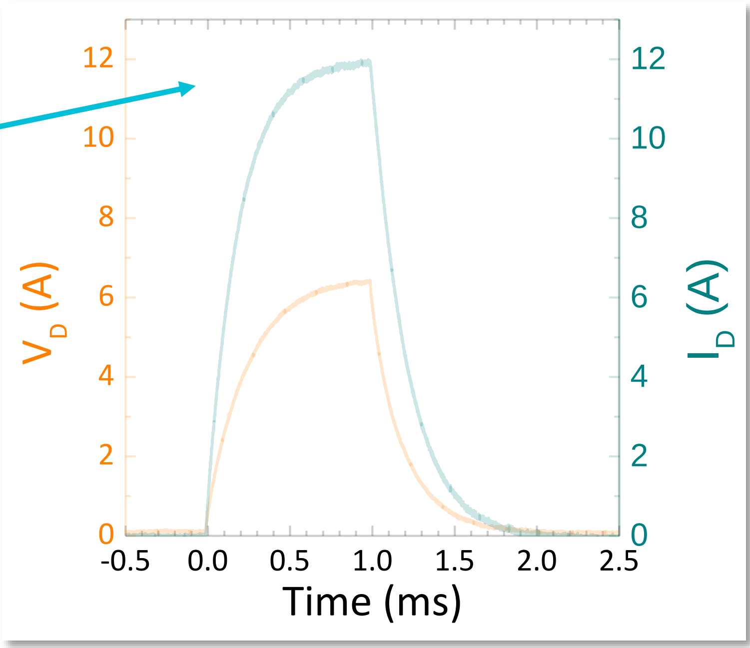
DC-measurement setup



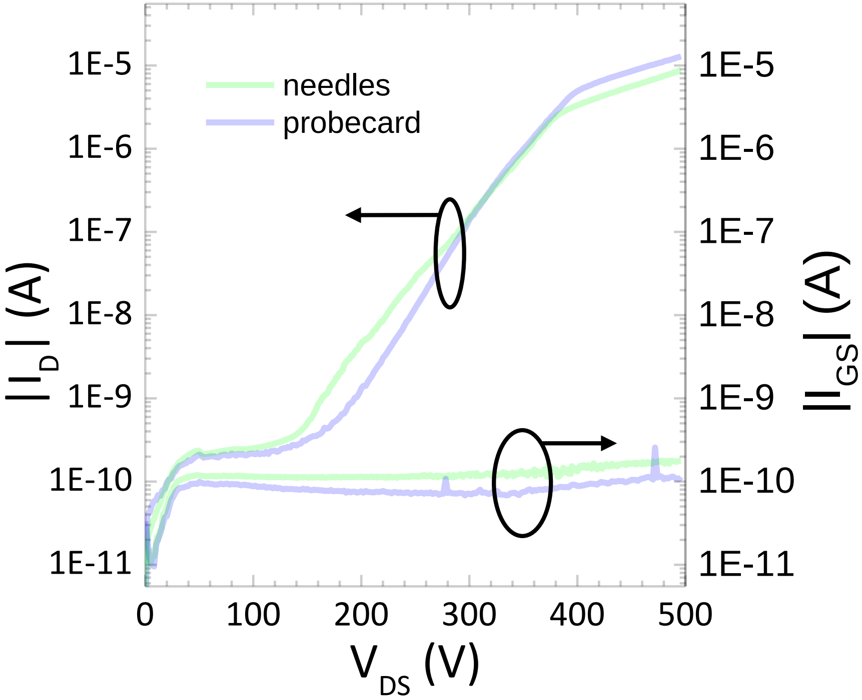
DC-measurements: I_D-V_{DS}

- Output current of an e-mode power devices
- Long-pulses (1ms pulse width, duty cycle 100%)
- Smooth shape of the measured curves





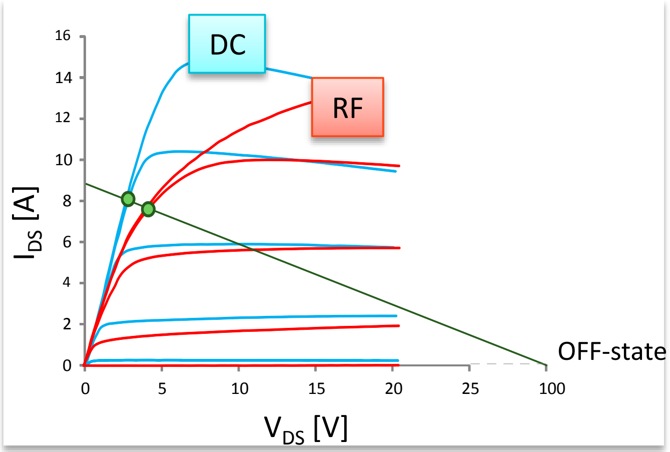
DC-measurement: leakage



- The probe card does not introduce additional leakage in the measurement

Trapping effect in GaN-HEMT

GaN technology is not immune to trapping effects. The most detrimental effect of traps for the device behavior is the decrease of the output current (increase of dynamic R_{DS-ON}). Traps in GaN-HEMT can be at the surface and in the buffer.

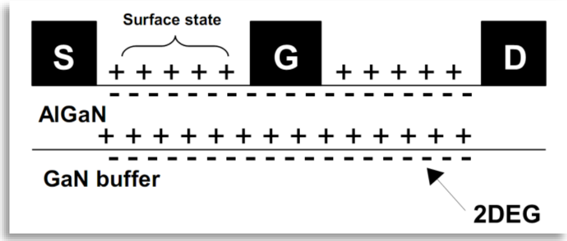


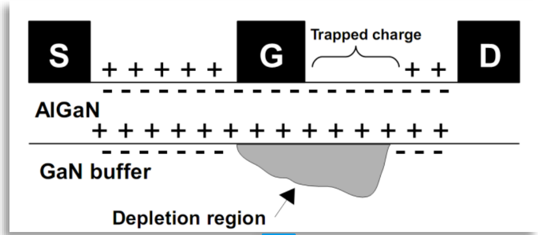
The effects of a higher R_{DS-ON} in a switching application are:

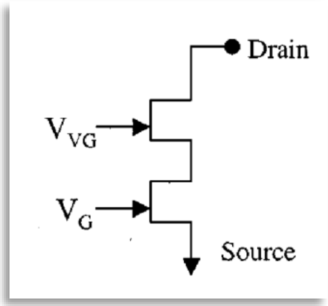
- Higher dissipative power on the transistor
- Higher T_j
- Increased power loss (lower efficiency)
- Distortion of the V_{out}

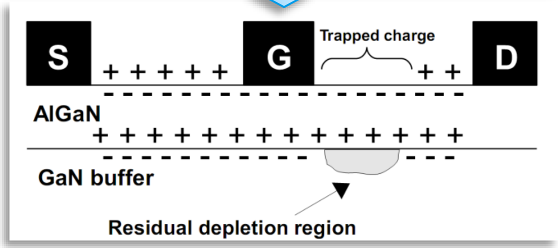
Virtual gate effect

The effect of surface traps is often compared to the presence of a "virtual gate" in series with the "real" gate.









The complete turn-on of the device is linked to the release of the trapped charge.

Vetury, R.; "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs"; IEEE Transactions on Electron Devices 2001

Avoid trapping in AlGaN/GaN HEMT

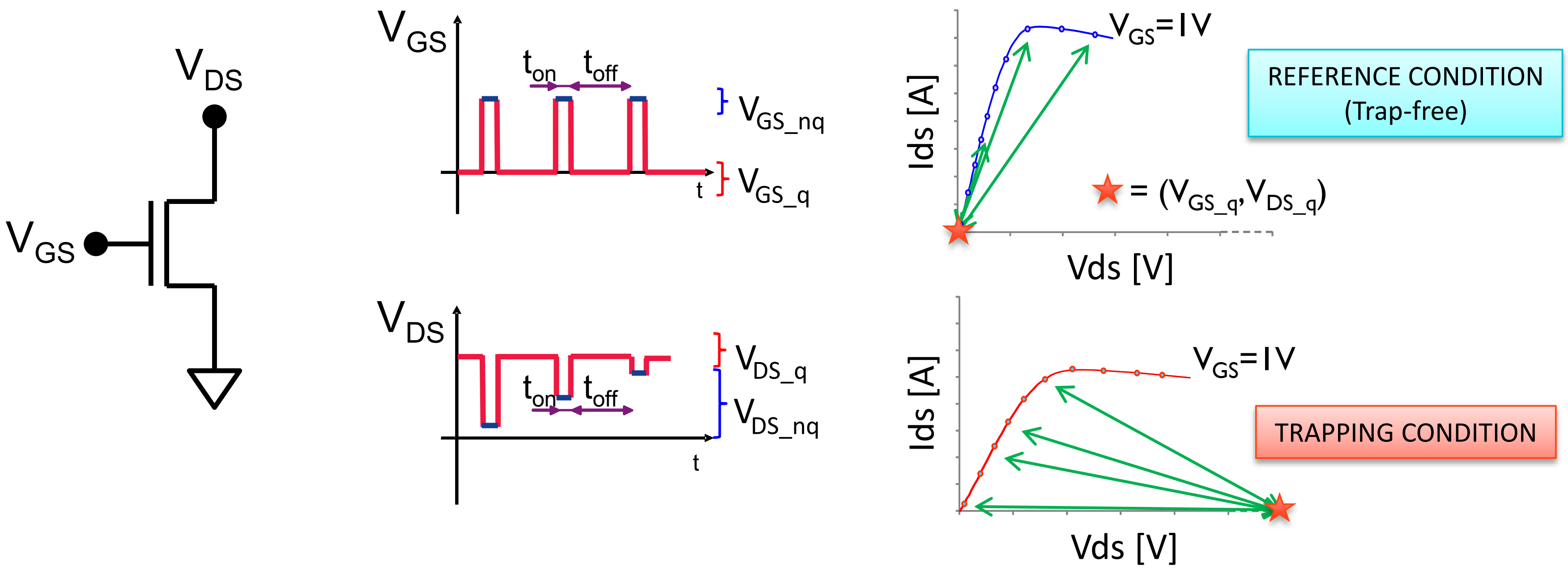
For a low dynamic $R_{DS\text{-}ON}$ dispersion, the following points have to be addressed:

- Improve the epitaxial layer quality (buffer-dispersion)
- Decrease the number of trapping states at the surface (passivation/surface cleaning)
- Decrease the intensity of the electric field peak (field plate)

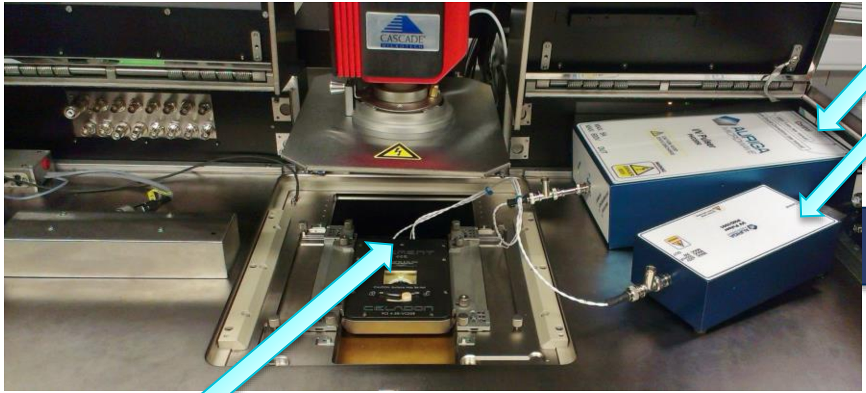
The dynamic $R_{DS\text{-}ON}$ must be measured in a reliable way and in a bias condition similar to the device targeted application.

Dynamic $R_{DS\text{-}ON}$ dispersion

The dynamic $R_{DS\text{-}ON}$ is measured from the I_D-V_{DS} characteristic by means of pulsed measurements (with high drain bias applied during the off-state).



Auriga P-IV system

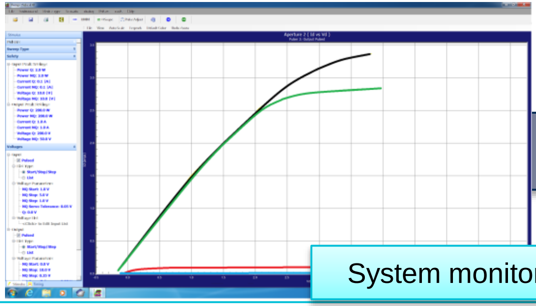


Drain “HEAD”

Gate “HEAD”

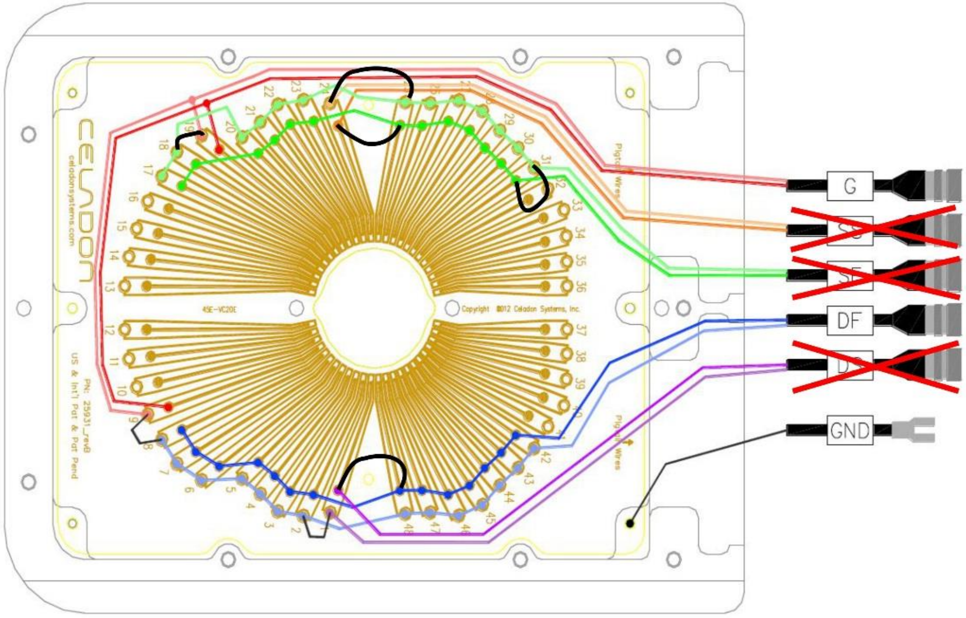
Short coax cables

AURIGA AU4850 mainframe



System monitor

Probe card connections

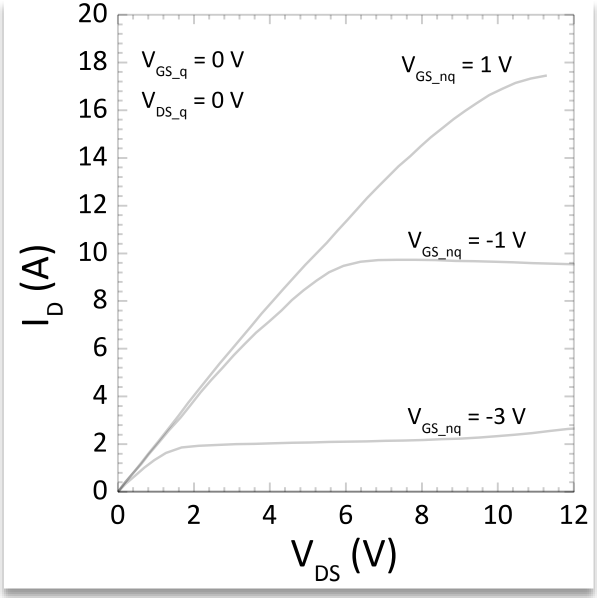


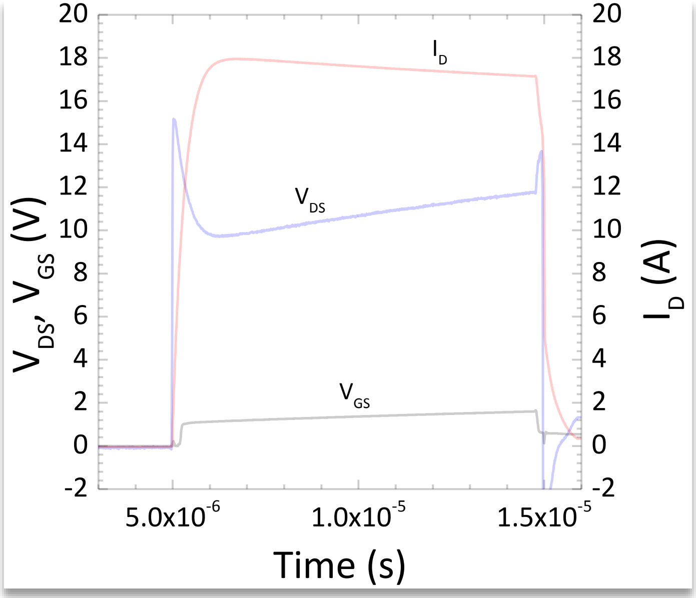
For fast switching measurements long current paths and ground loops must be avoided.

- Source connections are removed
- No sense terminals are needed
- The “return” of the current is through the shield of the drain cable

P-IV measurements

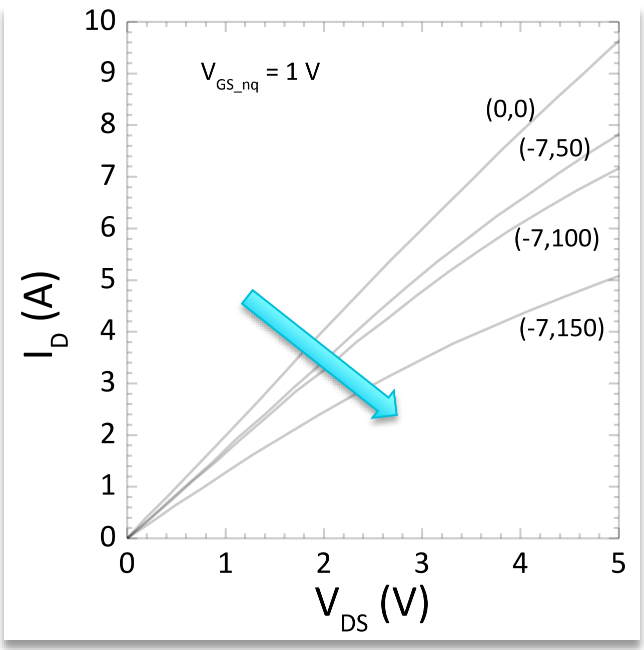
- Output current of a d-mode power devices
- Short-pulses (10 µs pulse width, duty cycle 10%)
- Limited amplitude of spikes (mainly due to the d-mode operation)

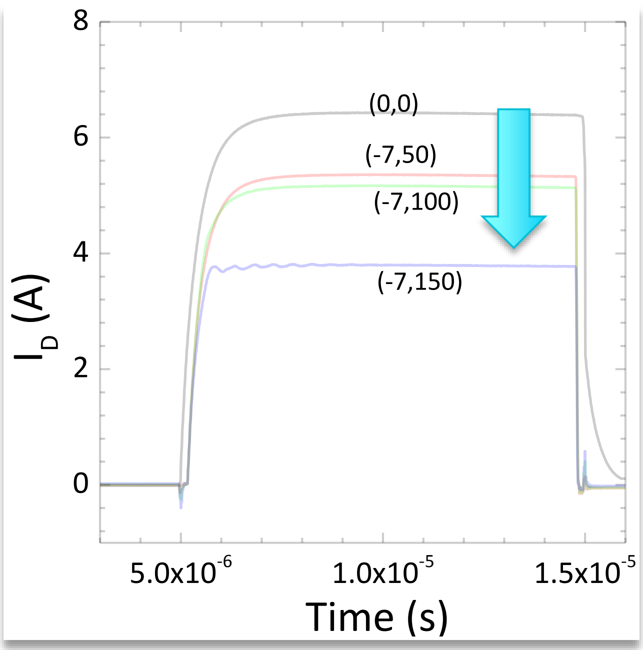




$R_{DS\text{-}ON}$ dispersion

- Dynamic $R_{DS\text{-}ON}$ degradation for high V_{DS_q}
- Limited amplitude of current spikes





Conclusions

In this presentation we have demonstrated how the CELADON VC20 VersaCore™ and the 45E probe card holder are successfully used for testing GaN power devices for switching applications.

In particular, we have shown:

- On-wafer high voltage and high current measurements
- Versatility of the interchangeable cores to match the device layout
- Smooth shape of the measured waveforms
- Reliable measurements of fast high-current pulses
- Limited spikes
- Easy to use and reproducible measurement setup

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