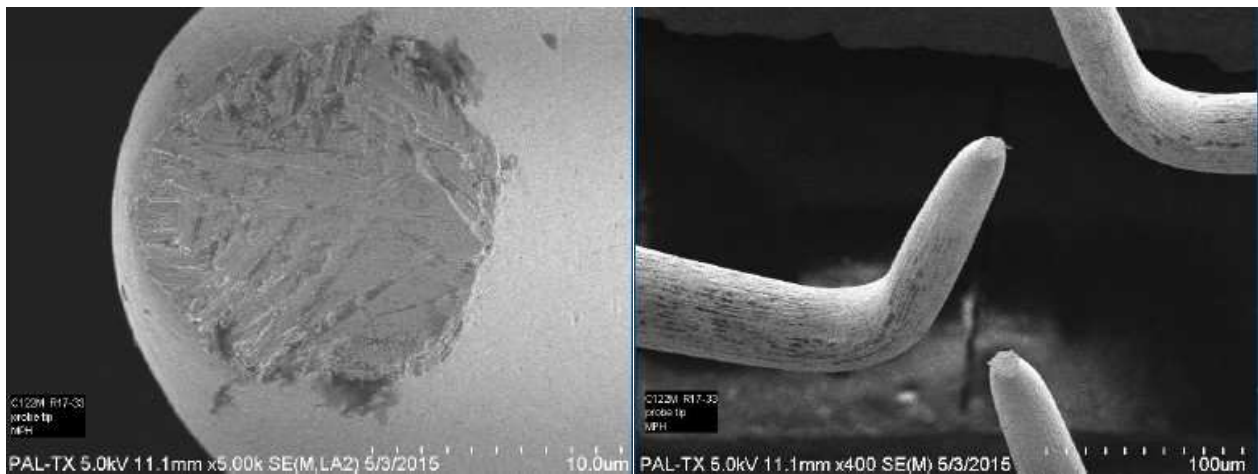


## Celadon Probe Cards and Products

### A Guide to Contact Resistance, Frequently Asked Questions, and Best Practices



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## 1 INTRODUCTION: WHAT IS CONTACT RESISTANCE, AND WHY DOES IT MATTER

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This guide provides information on Contact Resistance [Cres] as measured in ohms [ $\Omega$ ] from probe tip to bond pad on semiconductor wafers. Cres is an electrical quantity that measures how the contact area between the probe and the pad impedes the electrical flow.

Why is this important?

Low Cres helps preserve the electrical integrity of data collected. If Cres is not properly managed, it can cause offsets in data as well as increase the risk of melting probe tips.

Cres is also important to manage the lifetime of the probe tips on a probe card. In high current applications, if Cres rises due to embedded particles in the tip or oxidation, you are trying to push what previously was a manageable amount of power, through a smaller area. If Cres gets too high, the probe tip will be damaged, or melt completely, causing significant cost to repair the card.

Properly maintained probes will remain stable for test for a long time, but only if the correct cleaning recipe is used.

For the “Celadon Toothbrush” cleaning method, please follow the link below for off-line cleaning.

<https://www.youtube.com/watch?v=6lQT6TCs144>

## 2 FREQUENTLY ASKED QUESTIONS

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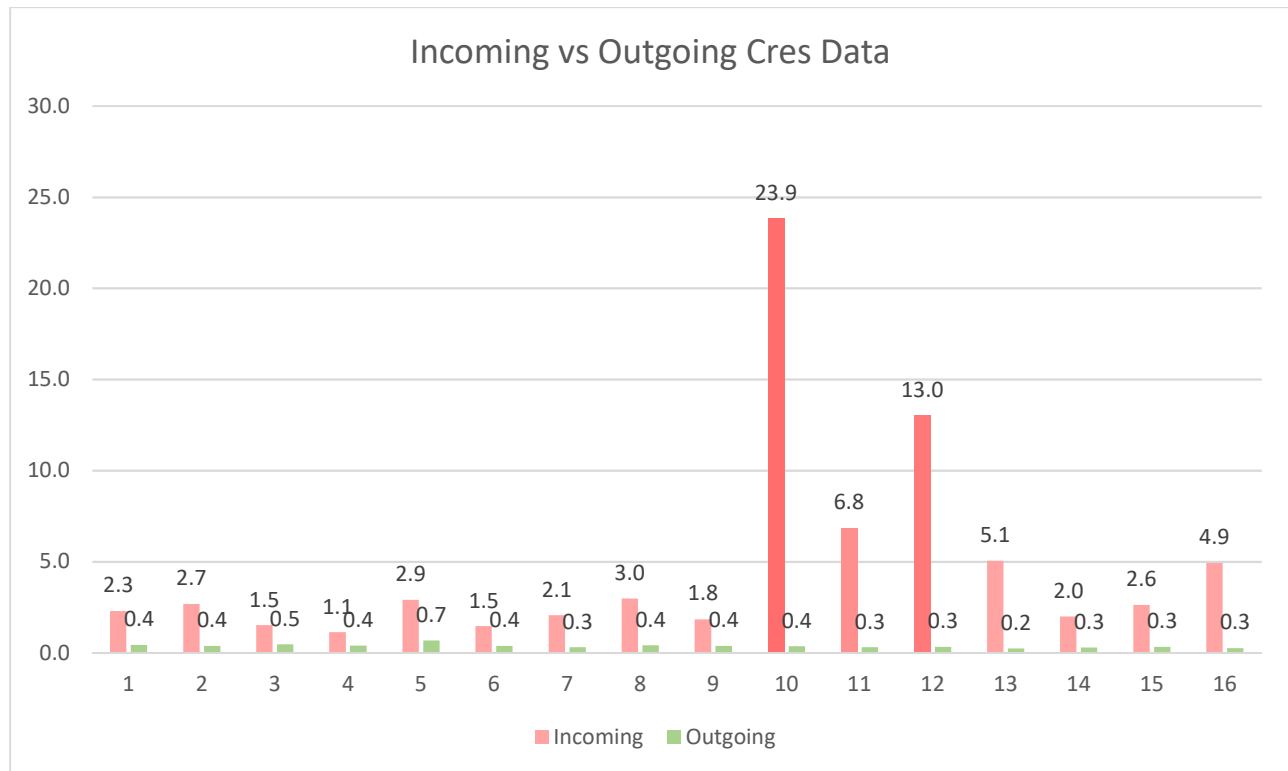
- What cleaning process should I use for my probe cards?
  - The exact process will vary significantly from customer to customer as tests, conditions, and wafer materials vary significantly. In short, Celadon Systems does have recommendations, but the exact cleaning recipe varies from customer to customer based on electrical test performed, lab environment, and wafer material.
- Will aggressive cleaning to manage cres decrease probe lifetime?
  - While the best way to manage Cres is a more aggressive cleaning substrate, when used properly in tandem with a less aggressive medium for standard cleaning, you can still obtain extreme probe life in Celadon probe cards.
- Is In-Situ [In-Line] cleaning sufficient to maximize the life of my probe card?
  - While Celadon probe cards are very robust, the optimal regiment for a probe card is a balance of: In-Situ cleaning using prober auxiliary chucks with cleaning substrates or cleaning wafers, off-line cleaning with Celadon toothbrush, and bi-annual Probe Maintenance [PM] at Celadon headquarters [details on PM service in section 3]. When properly maintained, Celadon probe cards are capable of reaching 10+ million touchdowns [ref:1].
- Does my offline cleaning alcohol effect the product?
  - Celadon has found that alcohol type can affect the electrical performance of probe cards and accessories. IPA can leave a residue that causes leakage and performance issues. Celadon recommends using semiconductor grade ethyl alcohol. “Denatured Ethyl Alcohol - Anhydrous 99% - Technical Grade NA-1987.
- Should I clean my motherboard PCB?
  - Spot cleaning 4062, 4062-80, and 4080 series motherboards is acceptable. Use a clean room cloth with Ethyl alcohol to spot clean, wipe off with clean room cloth and DI water, bake for 2hours at 80C. Do not fully submerge!

### 3 CONTACT RESISTANCE MANAGEMENT – BEST PRACTICES

The best way to keep your Cres low, is with proper probe maintenance. While the exact process and cleaning materials vary from customer to customer, Celadon recommends the following steps to help dial in cleaning.

**Problem:** High Cres after testing multiple wafer lots [normally cres doesn't increase with a single test, it is a slowly increasing value as more and more particle are embedded in the tip of the probe, degrading the electrical signal and impeding the current flow].

Below is actual test data taken from an incoming probe card with Cres issues in the field. Celadon took incoming Cres measurements on a blanket Al sputtered wafer.



After the card is received at Celadon the card goes through an alcohol and hot water bath, followed by clean air dry, then baked for 2-4 hrs. This bath/bake process of the PM cleans to manage leakage. The Cres management is accomplished by touching down the probe card on a Celadon Tungsten Carbide [CWC™] substrate or Celadon Tungsten Carbide Cleaning Wafer. For best results with Tungsten Carbide cleaning substrate **the overdrive used on the substrate should match that of your test environment.**



For In-Situ cleaning, we recommend ITS Probe Polish 99, the different part numbers are as follows for various systems.

TEL P8/P8E	PP-2001-9903SC/I-M, 2" 99% ITS
EG4085	PP-2010-9903SC/I-M, 1.5"x1.5 ITS
P8XL-LC	PP-2049-9903SC/I-M 4.25"
UF200	PP-2001-9903SC/I-M, 2" 99% ITS

Some production customers use probe polish as frequently as every 250-500 touchdowns/device contacts.

For ITS Probe Polish, touchdown up to 30 times in a step array, with at least 75 microns between steps. The stepping will prevent overuse of the gel pad that could result in picking up polish substrate particulate on the probes. Overdrive should be **over your normal test environment**, up to 100µm works well. The probe polish will also need to be changed on a regular basis.

When Cres gets too high, only then do you use a CWC™ plate or wafer to remove embedded particles and oxidation.

## 4 EXISTING CLEANING RECIPES FROM THE FIELD

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- **FACTORY 1:** Uses PP70. Cleans after every 175 touchdowns. Cleaning recipe is 15 touches. OD into cleaning material is 30µm [30µm on wafer]. They have been running 24/7 on Celadon cards since late 2016, and lifetimes are in excess of 5M touchdowns.
- **FACTORY 2:** Uses PP150. Cleans after every 60 touchdowns. Cleaning recipe is 10 touches. OD into cleaning material is 30µm [70µm on wafer]. (Our opinion is this recipe is possibly too aggressive – still being evaluated for lifetime performance)
- **FACTORY 3:** Does no cleaning inline at all. When they see a CRES increase, they pull the card and send it to the probe card repair shop for an offline “toothbrush clean”. Some cards that have been in use for months and years and never cleaned at all. This factory sees extremely long probe card life, but they have no way to count TD.
- **NXP - TX:** Use PP99. Cleans after every 350 touchdowns. Cleaning recipe is 30 touches. OD into cleaning material is 100µm [55µm OD on wafer] then touch prober brush on occasion.  
Every 100K TD, they do a cloverleaf pattern on a tungsten block. Lifetime in excess of 20M touchdowns.
- **LABS:** They tend to use aggressive cleaning media. One engineer likes Tungsten Carbide for WLR testing (10 taps into CWC™ block after each wafer, overdrive on CWC™ substrate is probing overdrive +1µm). All labs tend to be similarly aggressive with cleaning since lifetime is not a concern for them.

## 5 REFERENCES

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Ref 1: Production Parametric Test – Challenges and Surprising Outcomes Running in a High-Volume Manufacturing Environment [produced in partnership with NXP {formerly Freescale} and presented at SWTW 2015]

## 6 CONTACT INFORMATION

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## 7 REVISION HISTORY

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Revision	Changes	Date	Approval
1.0	Initial Release	6/27/17	GET
1.1	Updated to include UF200	7/25/17	GET
1.2	Recipes Added	10/6/17	GET
01.3	Misc Updates	11/6/17	GET
01.4	Added Lab Recipe	2/26/18	GET
01.5	Updated to CWC™	11/12/19	GET
01.6	Added notes on IPA	3/6/20	GET