DELPHON

Merging Innovative Technologies

Increasing the Role of Probe from Lab to Fab: The Mission of Critical Data

Jerry Broz, PhD

VP of Business Development & Strategic Marketing, Delphon Industries, LLC.

General Chair of SWTest Conferences

Gel-Pak®

Protecting the World's Valuable Devices

Outline

- Gel-Pak | Delphon Corporate Snapshot
- Semiconductor Landscape
- Mission of Probe
- Lab to Fab Challenges
- Summary and Takeaways

Gel-Pak | Delphon | At-A-Glance

Gel-Pak®
Protecting the World's Valuable Devices

Device Protection and Elastomer Film Solutions

TOUCHMARK
MEDICAL DEVICE PAD PRINTING

Specialty Printing and Coating Solutions

UltraTape
Adhesive Tapes and Labels for Critical Environments

Tapes and Labels for Cleanroom Environments

Merging Innovative Technologies

DELPHON

- Delphon Industries develops and delivers highly engineered materials for the semiconductor, medical, photonics, and electronic industries.
- High volume, ISO 9001:2015 certified facilities are headquartered in Hayward, CA with operations in Wilsonville, OR, and Johor, Malaysia.
- With 90,000 sq. ft. and several ISO Class 7 cleanrooms, Delphon Divisions have been producing innovative products since 1980.
- Over 1,000 global customers, ranging from Fortune 500 companies to startups to universities labs rely on Delphon expertise and innovation.
- Trusted by numerous industries to handle, transport, or process small, high value devices without risk of damage.

Evolving with Semiconductor Industry Trends

- Gel-Pak has continuously innovated to align with emerging trends in the semiconductor industry to address demanding applications.

1980

Beam Lead Diode was introduced to improve high-frequency performance and facilitate automated assembly

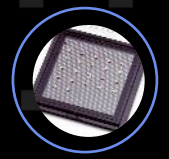
GEL-BOX

Gel-Pak partners with HP to create solutions for shipping beam lead diodes

Gel-Box was born

1990

Multi-Chip Modules introduced to enhance signal performance, reduce costs, improve flexibility, and reduce footprint.



VACUUM RELEASE (VR) TECHNOLOGY

Gel-Pak launches patented Vacuum Release Tray to drive Multi-Chip Module assembly efficiency.

2000

Thinner compound semiconductors improve performance, reduce power consumption, and enable miniaturization

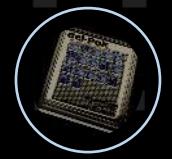
LARGE FORMAT VR NANO DEVICE TRAYS

Gel-Pak introduces large format carriers for thin compound semi wafers and substrates up to 300 mm.

NDT products for thin, ultra-small devices > 25 µm.

Mid 2000

Miniaturization trends introduce semiconductor reliability challenges and quality standards are elevated.



VERTEC® CARRIERS

Gel-Pak static dissipative, silicone-free Vertec carriers are introduced.

TODAY

Innovations in heterogenous packaging to overcome Moore's law drives advancements in semiconductor test.

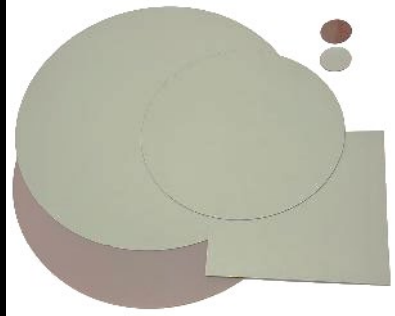
GEL-PROBE AND BTXF TEXTURED CARRIERS

Gel-Pak introduces textured device carrier ideal for in-process handling during heterogeneous integration.

Gel-Probe products improve wafer yield and reduce cost of test.

Gel-Pak Innovations Drive OEE

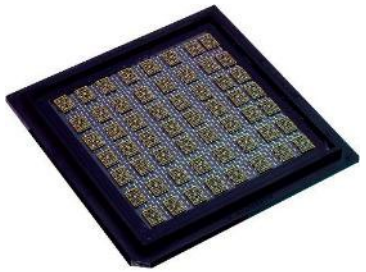
ELASTOMER PROBE CARD CLEANING FILMS



Gel-Probe Card Cleaning

- Custom coating of highly engineered elastomer films for semiconductor applications.
- Customizable probecard cleaning wafer and cleaning sheet applications.

SMALL DIE SHIPPING & HANDLING



Vacuum Release Carriers

- Automated pick & place applications for bare die and devices ranging from <250 micron to 75mm in size.
- Handling small components or large assembled modules.
- Suitable for transport and handling MEMs Probes

DIE WAFER & PANEL SHIPPING & HANDLING

Large Substrate Vacuum Release Carriers™

- Shipping and handling full or partial wafers, panels, and OTHER substrates from 75mm to 450mm.
- Suitable for KGD, singulated die, and film frame loaded devices.

UNIVERSAL & POCKETLESS CARRIERS

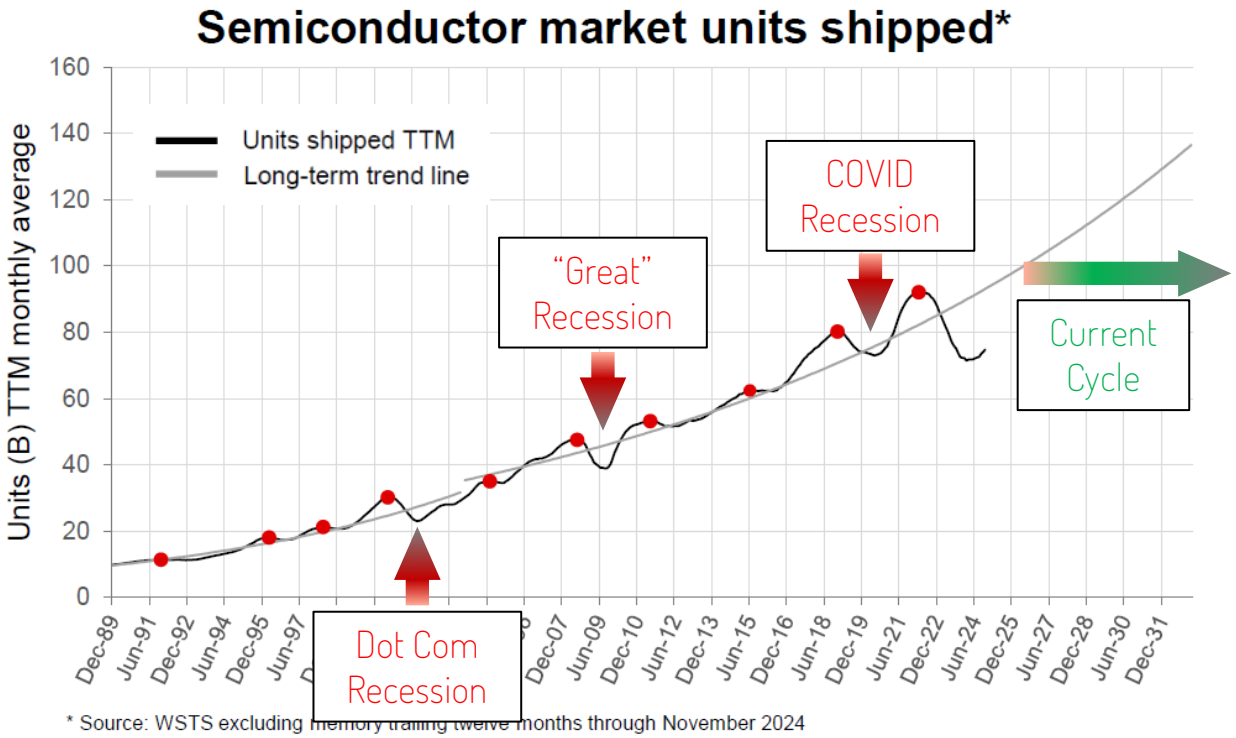
Textured Device Carrier Products

- Pocketless \carriers and transport products for KGD and other devices
- Universal Fixture for device handling in-process, singulated die testing, and shipping.

Outline

- Gel-Pak | Delphon Corporate Snapshot
- Semiconductor Landscape
- Mission of Probe
- Lab to Fab Challenges
- Summary and Takeaways

Semiconductor Is Notoriously Cyclical

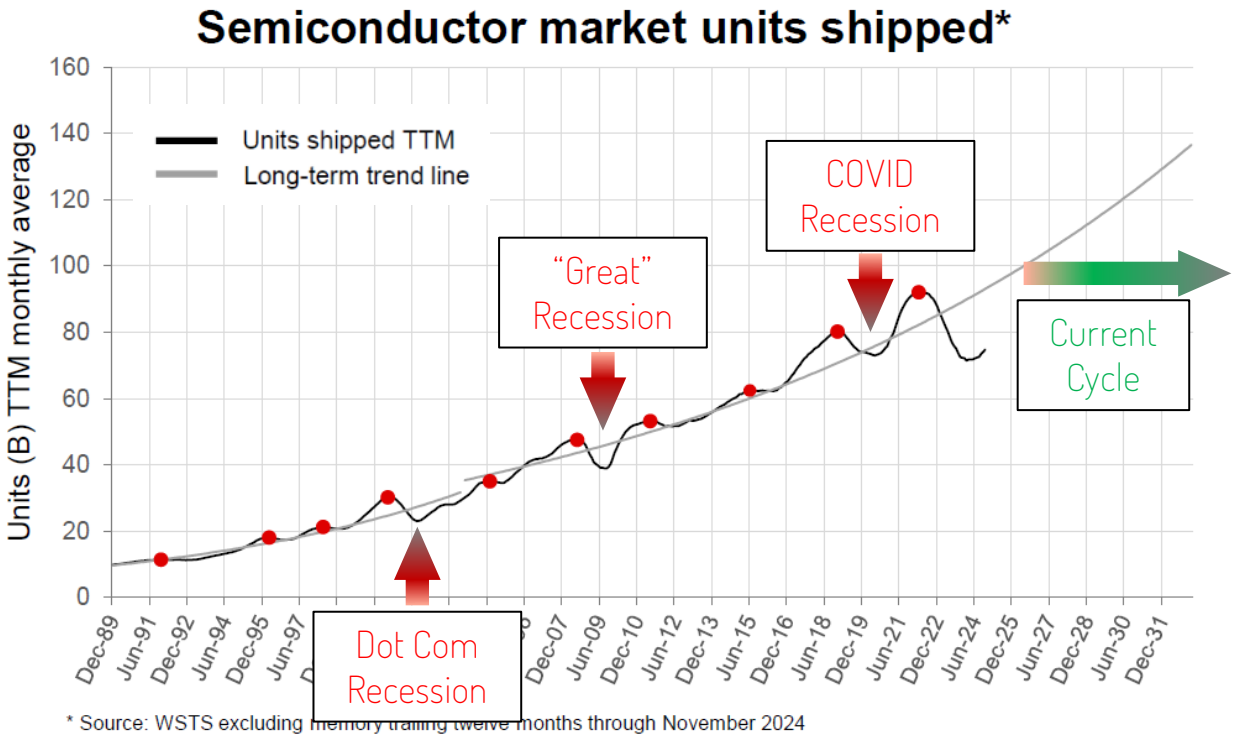


Factors in play:

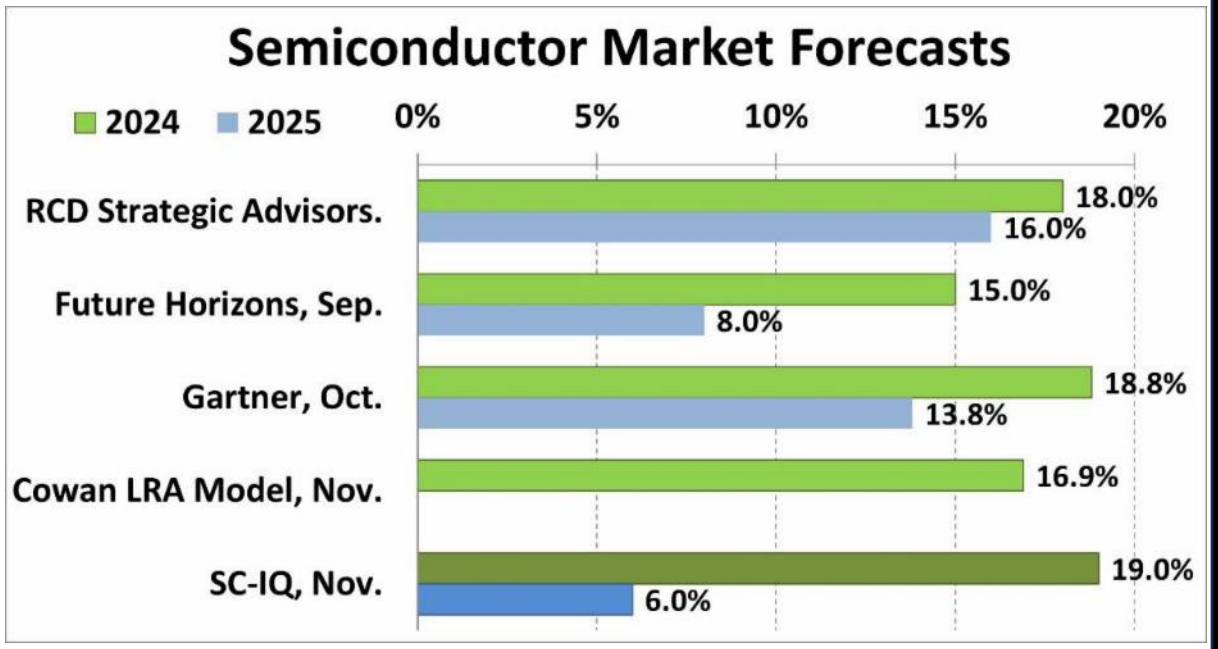
- **Third-quarter 2024 saw a semiconductor market growth of $166 billion, marking a 10.7% increase from the previous quarter and 23.2% year-over-year growth.**
- **Outlook for Q4 2024 indicates diverging trends, with strong AI-driven demand for data centers boosting revenues for companies like Nvidia, while automotive is forecasting declines.**
- **2025 projections show a mixed outlook with continued growth in AI, moderate growth in PCs/smartphones, and a weak automotive market, alongside potential consumer demand impacts from higher tariffs.**

Source: Texas Instruments Investor Day - 2024

Semiconductor Is Notoriously Cyclical



Factors in play:



Source: Texas Instruments Investor Day - 2024

Market Drivers

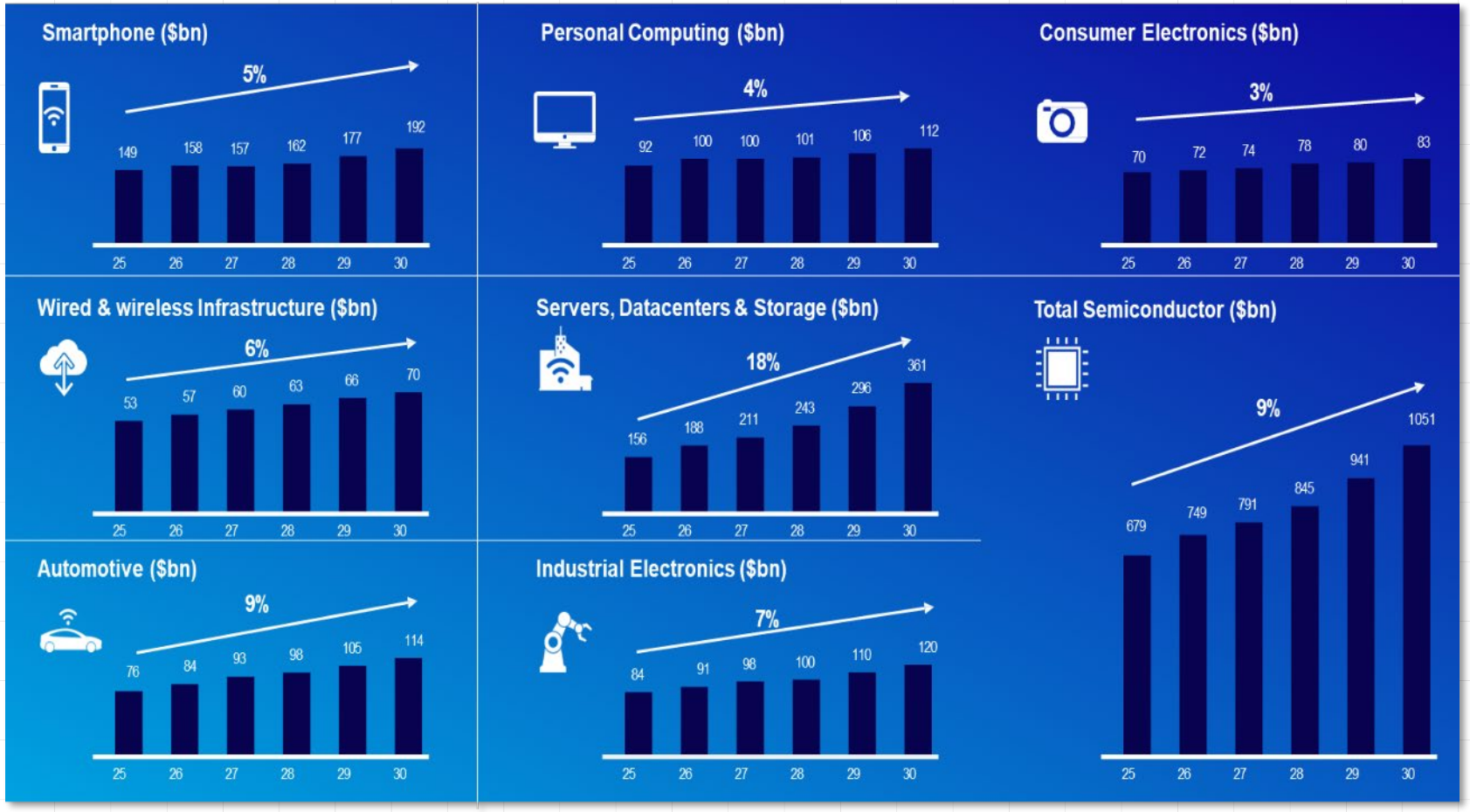
Data Cloud and AI
High-Capacity Storage, and HPC growing from 5 Zettabytes to > 40 Zettabytes

5G and Massive Connectivity
More than 1.1 billion smart-device and high-volume connections

Smart Devices
More than 250 million wearables and high-performance devices

Internet of Things
50B connected devices of low-cost devices and massive data volumes

Automotive Electronics
89 million connected cars each generating and processing > 1GB of data per second

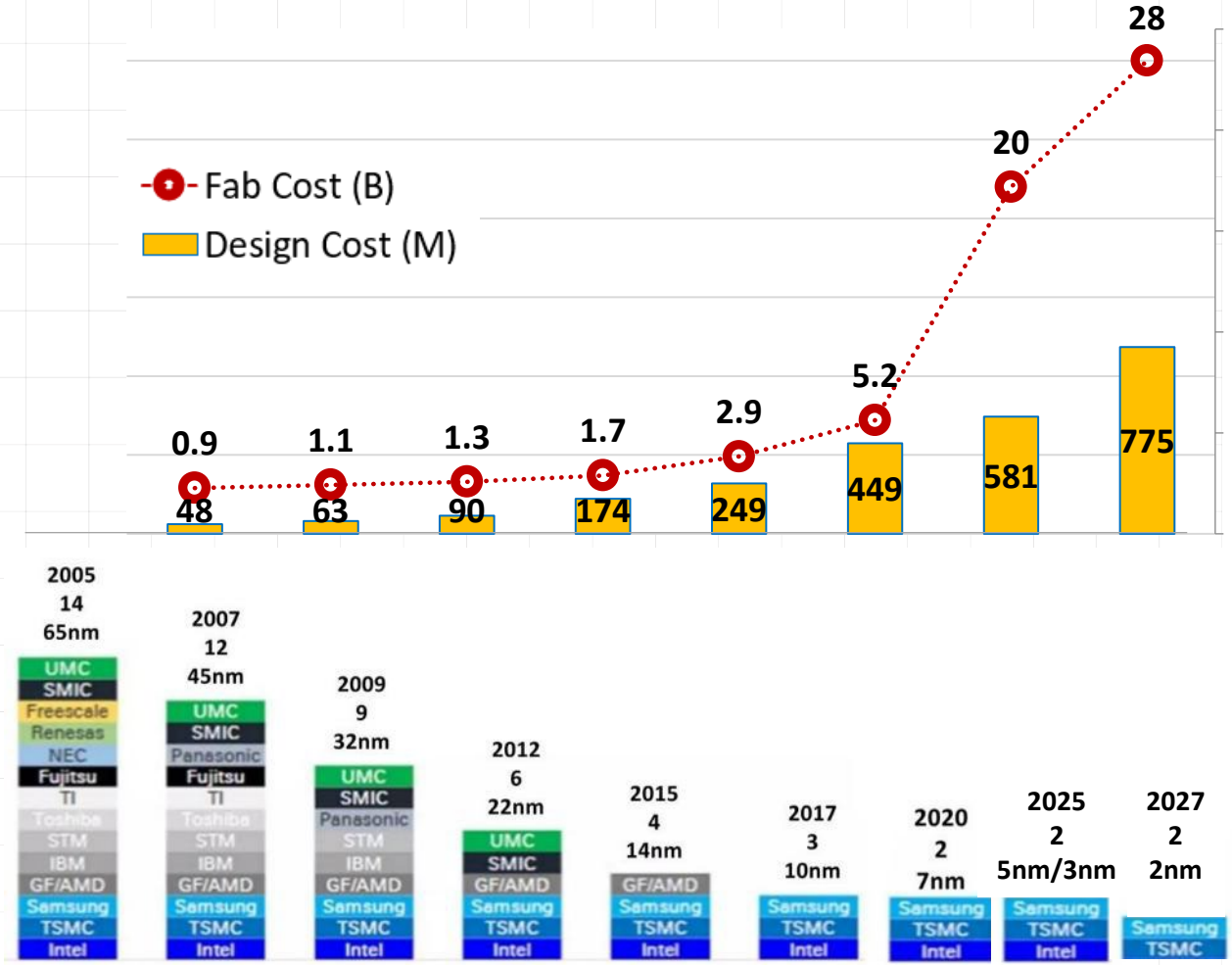


Process Everything | Store More Data | Compute Faster

Source: A. Harchandani, ASML Investor Day 2024

Costs of Accelerating Innovation

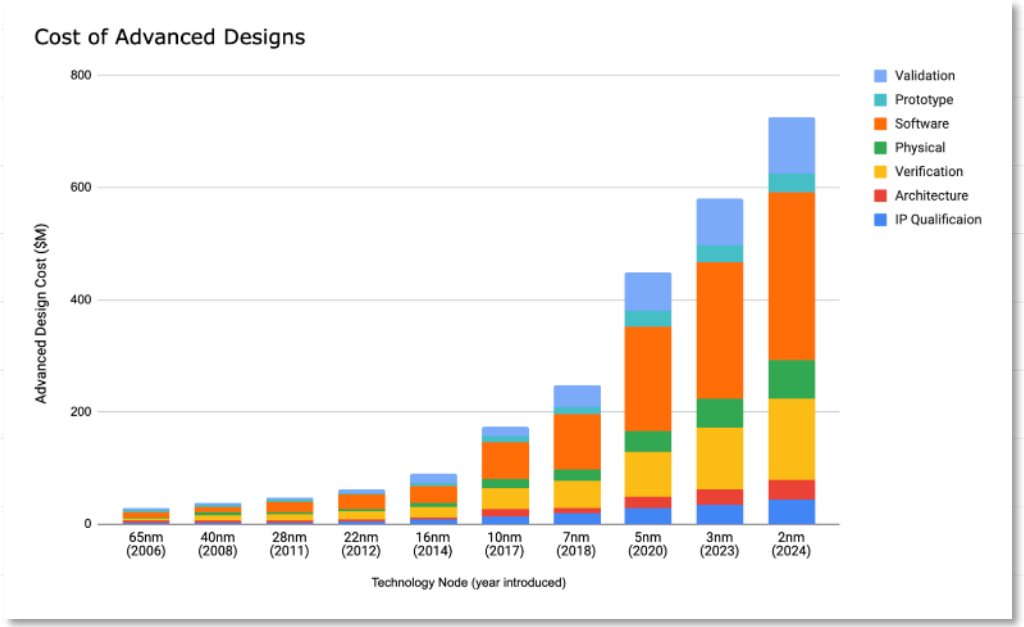
- Costs associated with design, introduction, and fab of new products for nodes below 22nm has increased almost 8X.
- "Monolithic" approach has extremely high development costs and precludes all but two global IDMs from pursuing this path.
- Heterogeneous integration and advanced packaging can use "best-in-class technologies" from multiple sources to advance performance trends at acceptable costs.
- Reuse of various designs can significantly lower costs when using standardized IP.



Source: Yole Intelligence, AMKOR, Semi-Wiki , IBS, KLA

Costs of Accelerating Innovation

- Costs associated with design, introduction, and fab of new products for nodes below 22nm has increased almost 8X.
- "Monolithic" approach has extremely high development costs and precludes all but two global IDMs from pursuing this path.
- Heterogeneous integration and advanced packaging can use "best-in-class technologies" from multiple sources to advance performance trends at acceptable costs.
- Reuse of various designs can significantly lower costs when using standardized IP.



Source: Yole Intelligence, AMKOR, Semi-Wiki , IBS, KLA

Consumer Demand

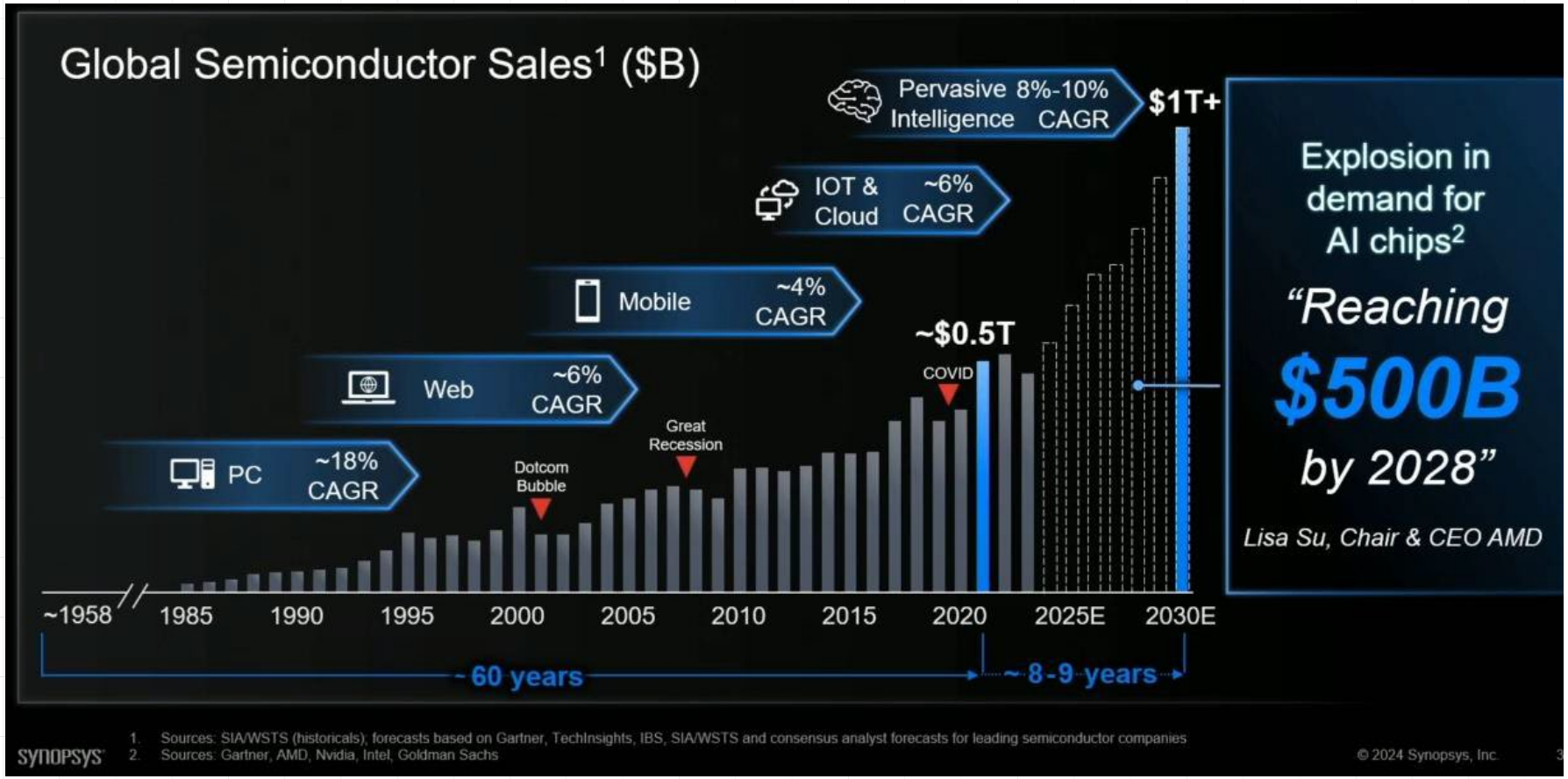
Data Cloud and AI
High-Capacity Storage, and HPC growing from 5 Zettabytes to > 40 Zettabytes

5G and Massive Connectivity
More than 1.1 billion smart-device and high-volume connections

Smart Devices
More than 250 million wearables and high-performance devices

Internet of Things
50B connected devices of low-cost devices and massive data volumes

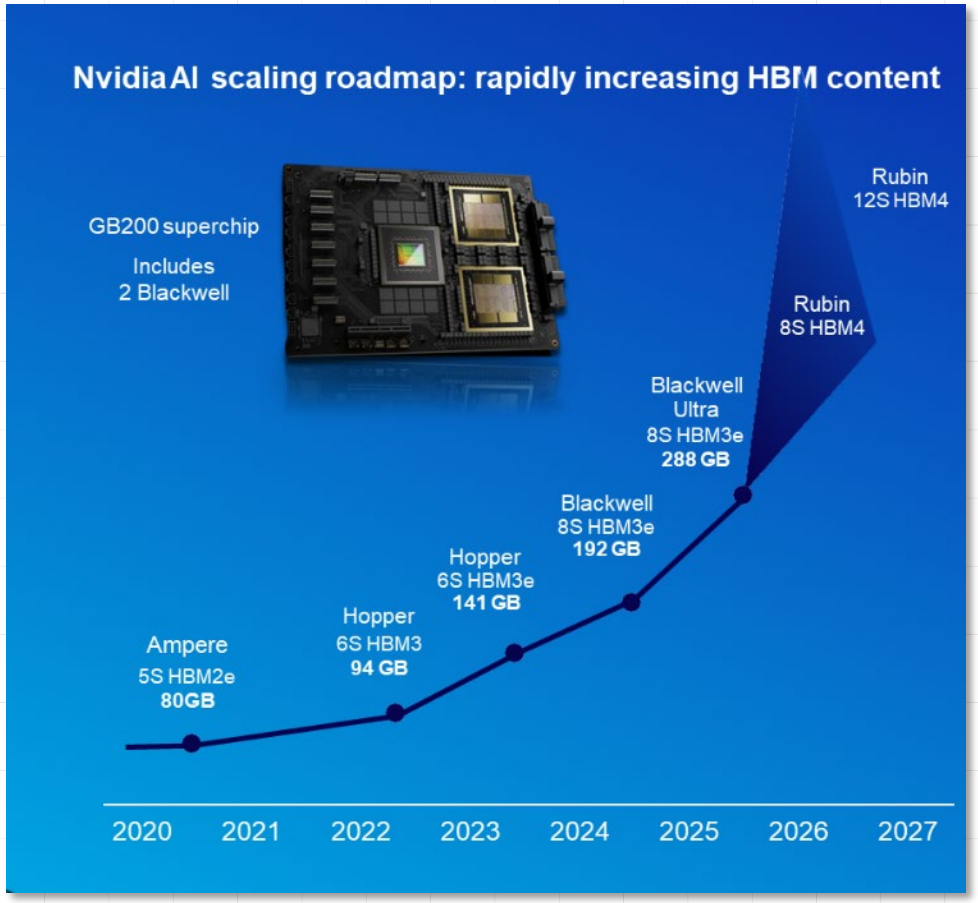
Automotive Electronics
89 million connected cars each generating and processing > 1GB of data per second



Process Everything | Store More Data | Compute Faster

Source: S. Kirshnamoorthy, IEEE ITC 2024

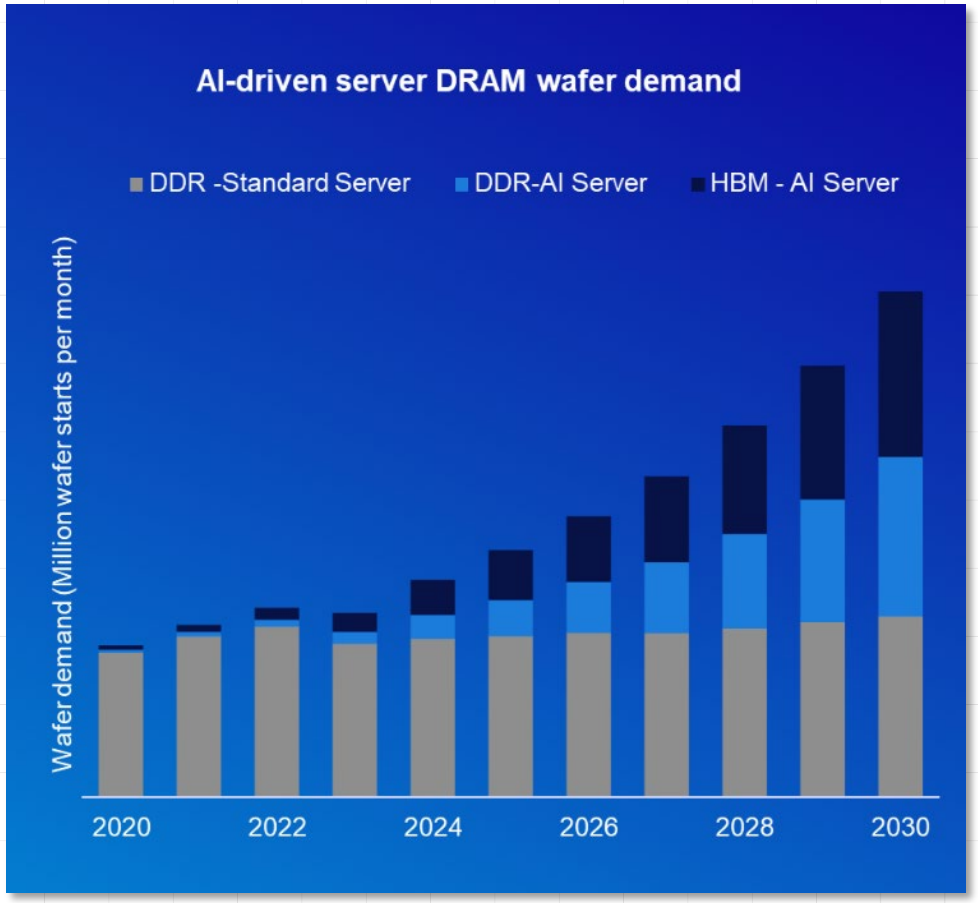
Demand for HBM & AI

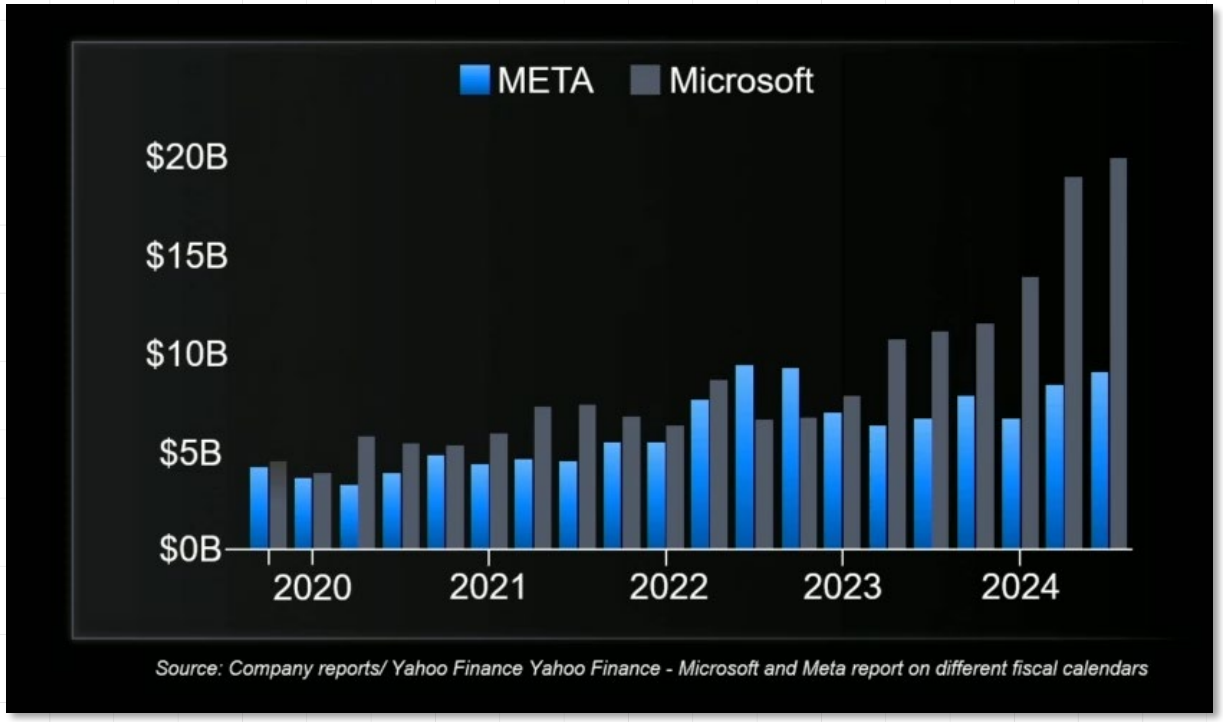


- **Global semiconductor sales hit $627.6B in 2024**
  - Increase of 19.1% over 2023 total of $526.8B.
- **Memory had 71.8% revenue growth in 2024.**
  - Memory's share as a percentage of total semiconductor sales increased to 25.2% in 2024.
  - DRAM revenue improved 75.4% in 2024 while NAND revenue increased 75.7% year-over-year.
- **Nonmemory revenue increased 6.9% in 2024.**
  - Nonmemory accounted for 74.8% of total semiconductor revenue in 2024.
- **High-bandwidth memory (HBM) production contributed significantly to DRAM revenues.**
  - HBM was 19.2% of DRAM Revenue in 2025 (up 13.6% over 2024)
  - HBM revenue is estimated to increase 66.3% in 2025, reaching $19.8B.

Source: ASML 2024 Investors, Yole Intelligence, Semi-Wiki , IBS

AI Demand & Expenditures





Memory and AI semiconductors will drive near-term growth, with HBM projected to account for an increasing share of DRAM revenue, reaching 19.2% in 2025.

Source: ASML 2024 Investors, S. Kirshnamoorthy, IEEE ITC 2024

Wafer capacity | Global Investments

US CHIPS and Science Act

- $52bn investment
- Tax credits
- Intel $40B
- TI $41B
- Micron $35B
- Wolfspeed $5B

European Chips Act

- $48bn investment
- Tax credits
- Infineon $6B
- Bosch $3B
- ASML $0.5B/yr

SOUTH KOREA-Semi Strategy

- Government support via tax credits and loans
- Samsung $230B
- SK Hynix $11B

JAPAN Strategy for Semi

- $26bn investment
- Tax credits
- SONY $7B

CHINA "Big Fund" Phase 3

- $48bn central government investment

INDIA Semiconductor Mission

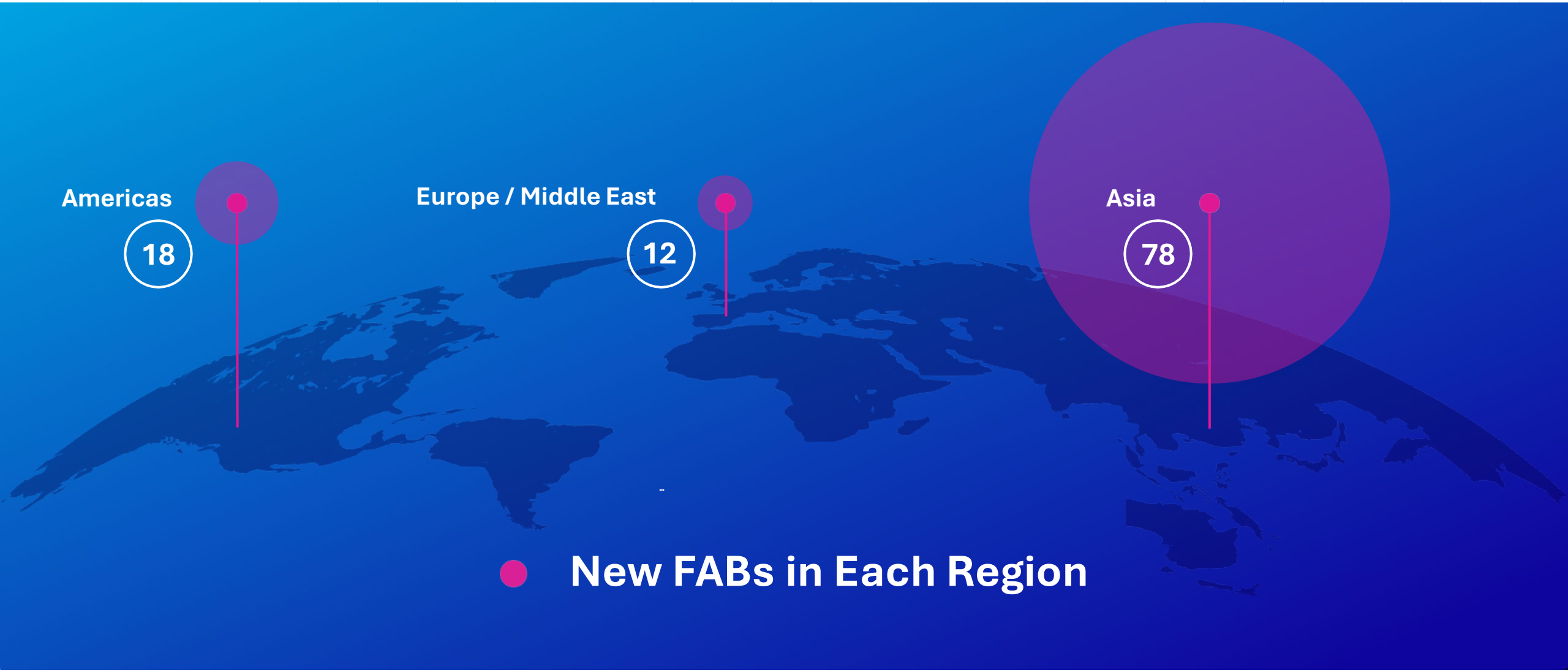
- $10bn government investment

TAIWAN Chip-Based Industrial Innovation Program

- $9bn investment
- Tax credits
- TSMC $100B
- UMC $15B

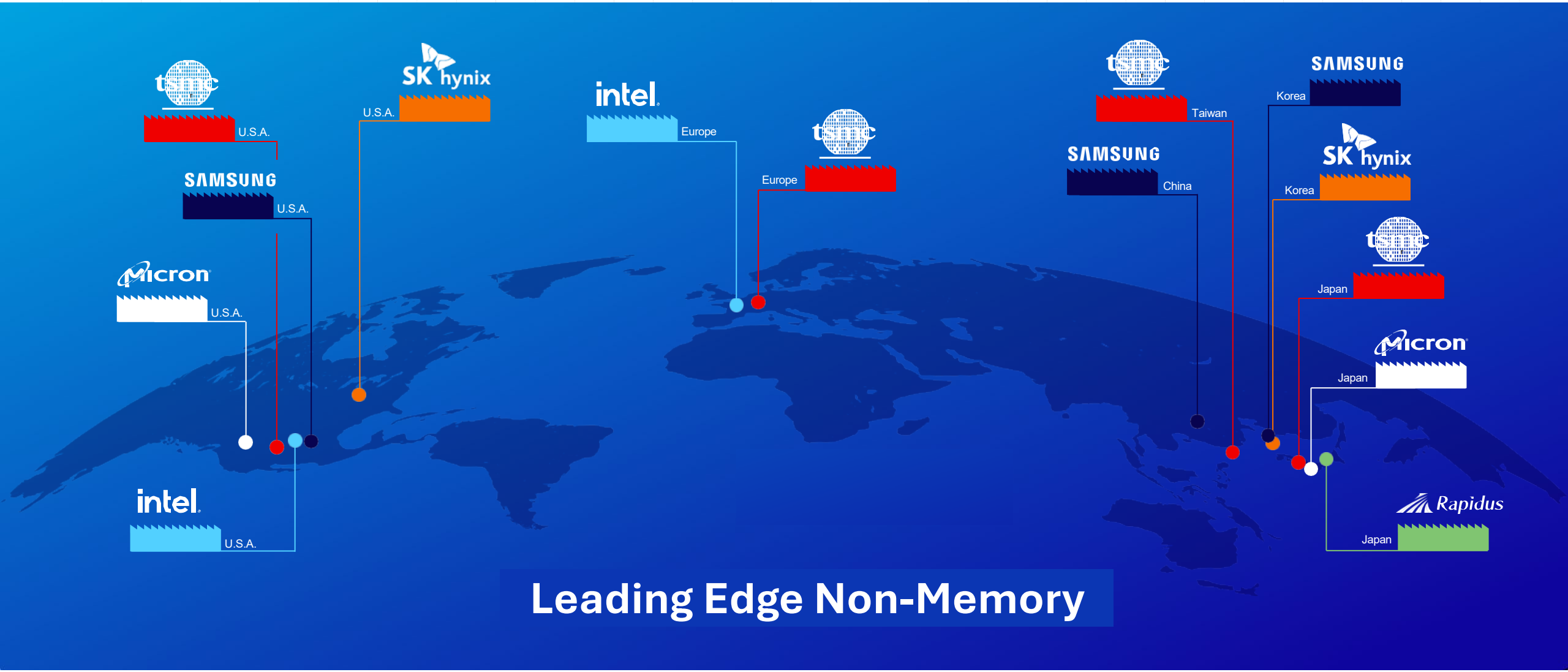
Government & Industry Investment

Wafer capacity | Global Investments



Source: SEMI.org, Public announcements, FTI Consulting analysis and ASML analysis; Note: The overview is not exhaustive

Wafer capacity | Global Investments



Source: SEMI.org, Public announcements, FTI Consulting analysis and ASML analysis; Note: The overview is not exhaustive

Outline

- Gel-Pak | Delphon Corporate Snapshot
- Semiconductor Landscape
- Mission of Probe
- Lab to Fab Challenges
- Summary and Takeaways

Mission of Probe is Critical Data

Image Source: Verigy

THREE PRIMARY COMPONENTS of a TEST CELL

1. **ATE**: Instruments & power supplies that stimulate and interrogate the DUT(s).
2. **Probe card**: Device-specific interface that provides the electromechanical DUT-to-ATE contact.
3. **Prober**: device wafer handling, positioning, thermal environment, and probe cleaning.

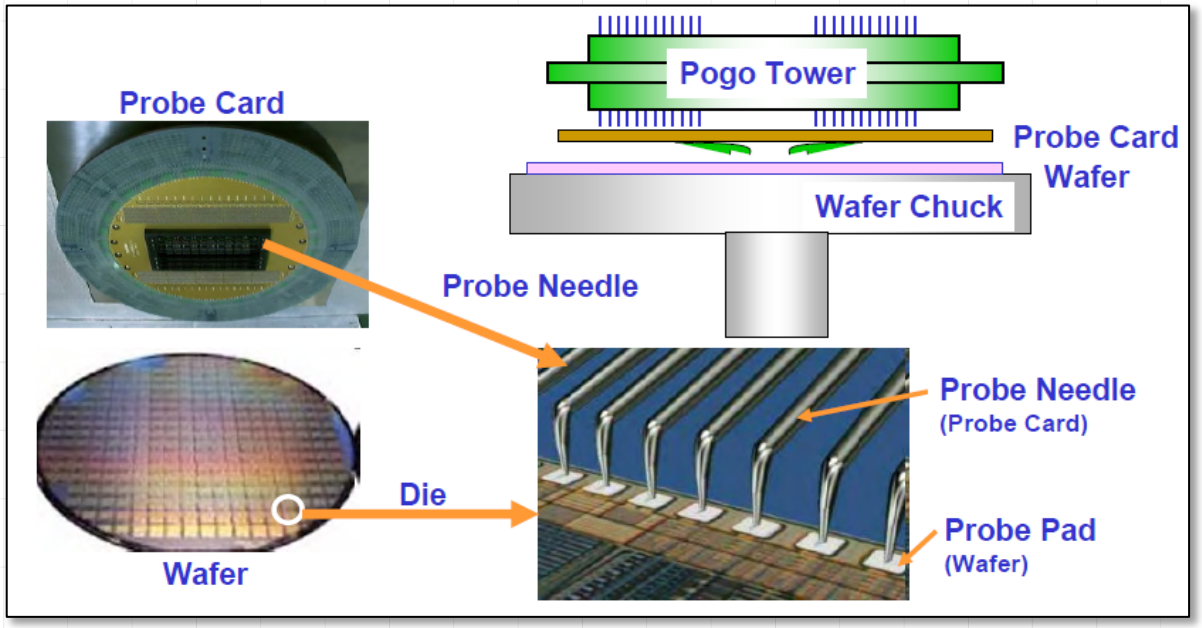
- **Feedback to FAB** for Manufacturing
- Reliable Data to **Improve Design**
- **Categorize Devices** on Performance
- **Maintain High Yields** to Avoid Retest
- Facilitate **Multi-Die "KGD" Solutions**
- **Reduce Yield Loss** at Final Test

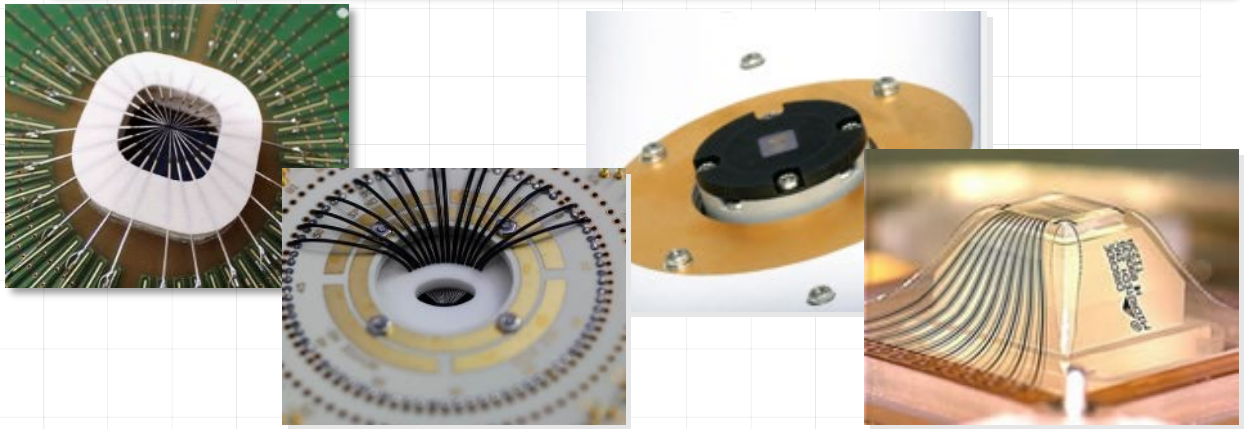
Test Provides Metrology For Entire Semiconductor Value Chain

Source: Ozawa, SWTest Asia 2019 Keynote, J. Broz, IEEE CISTIC 2020 Virtual

Probing is a “Contact Sport”!

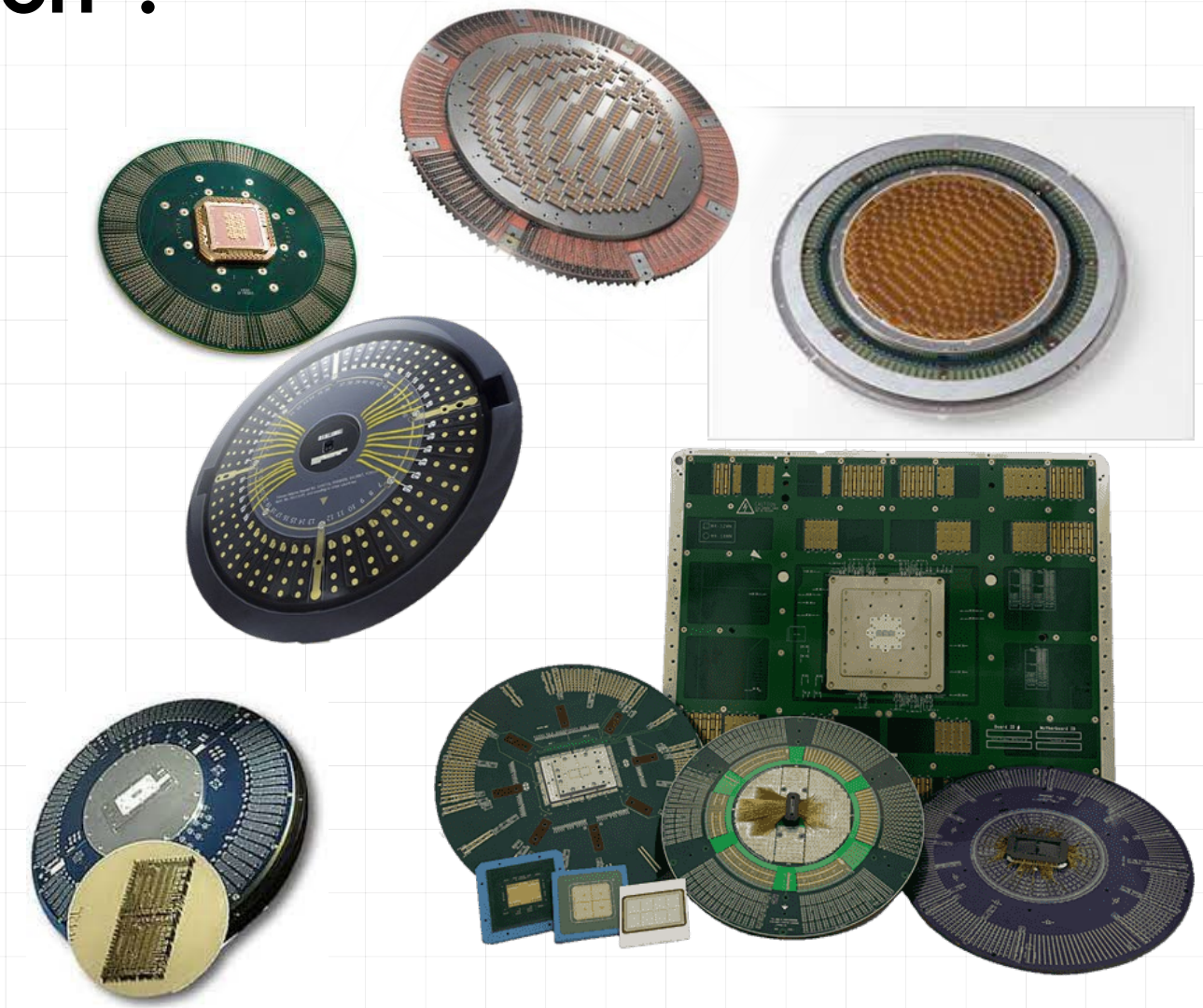
- Physical contact by small diameter probes onto the I/Os of individual DUTs.
- Electrical contact to execute various functional tests to determine the “goodness” of the device.
- Parametric test with low leakage, fast settling times, low cross-talk, guarded traces, temperatures from -55C to 200C.
- Production level memory and non-memory probe-cards are highly specialized for every application.





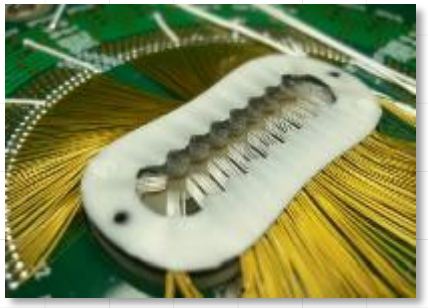
Probing is a “Contact Sport”!

- Physical contact by small diameter probes onto the I/Os of individual DUTs.
- Electrical contact to execute various functional tests to determine the “goodness” of the device.
- Parametric test with low leakage, fast settling times, low cross-talk, guarded traces, temperatures from -55C to 200C.
- Production level memory and non-memory probe-cards are highly specialized for every application.



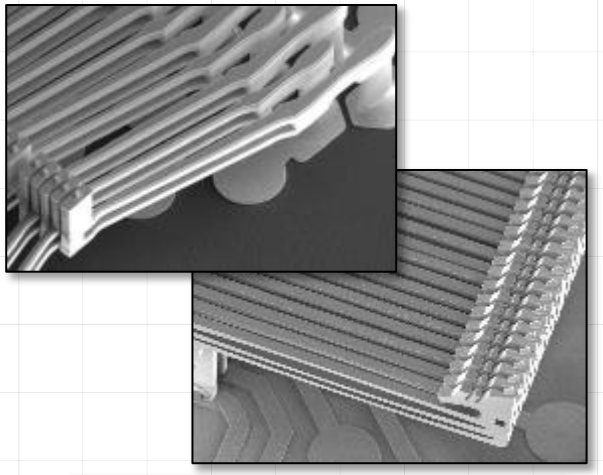
Probes Make the "Contact"

- **IC – Cantilevered Wire Probe**
  - Small diameter Tungsten, Tungsten Rhenium, BeCu wire probes mounted on a PCB.
  - Pin count range: tens up to several thousand.
- **IC - Vertical Probe**
  - Buckling beams, wired, or spring probes controlled using various guide plates.
  - Pin in count range: several thousand to more than 50K.
- **IC - MEMS Probe**
  - 3D MEMS : entire card (or tile) of multiple contacts are created as a single processed unit.
  - 2D MEMS : litho and etch processes to manufacture individual probe structures mounted onto a substrate.
  - Pin count range: several thousand to more than 200K.

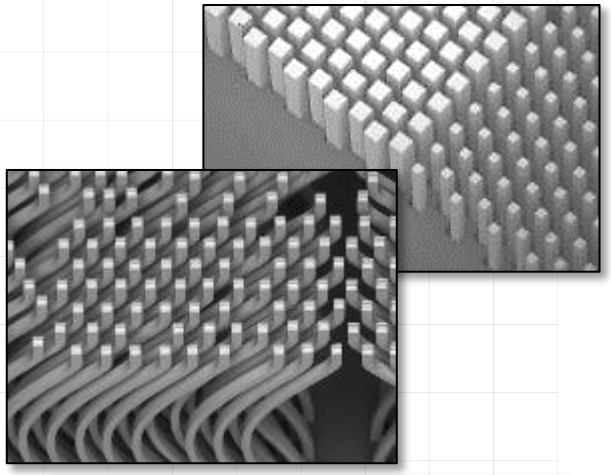


Cantilevered Probes
For Pads

Vertical Spring Pins
For Bumps and Pillars

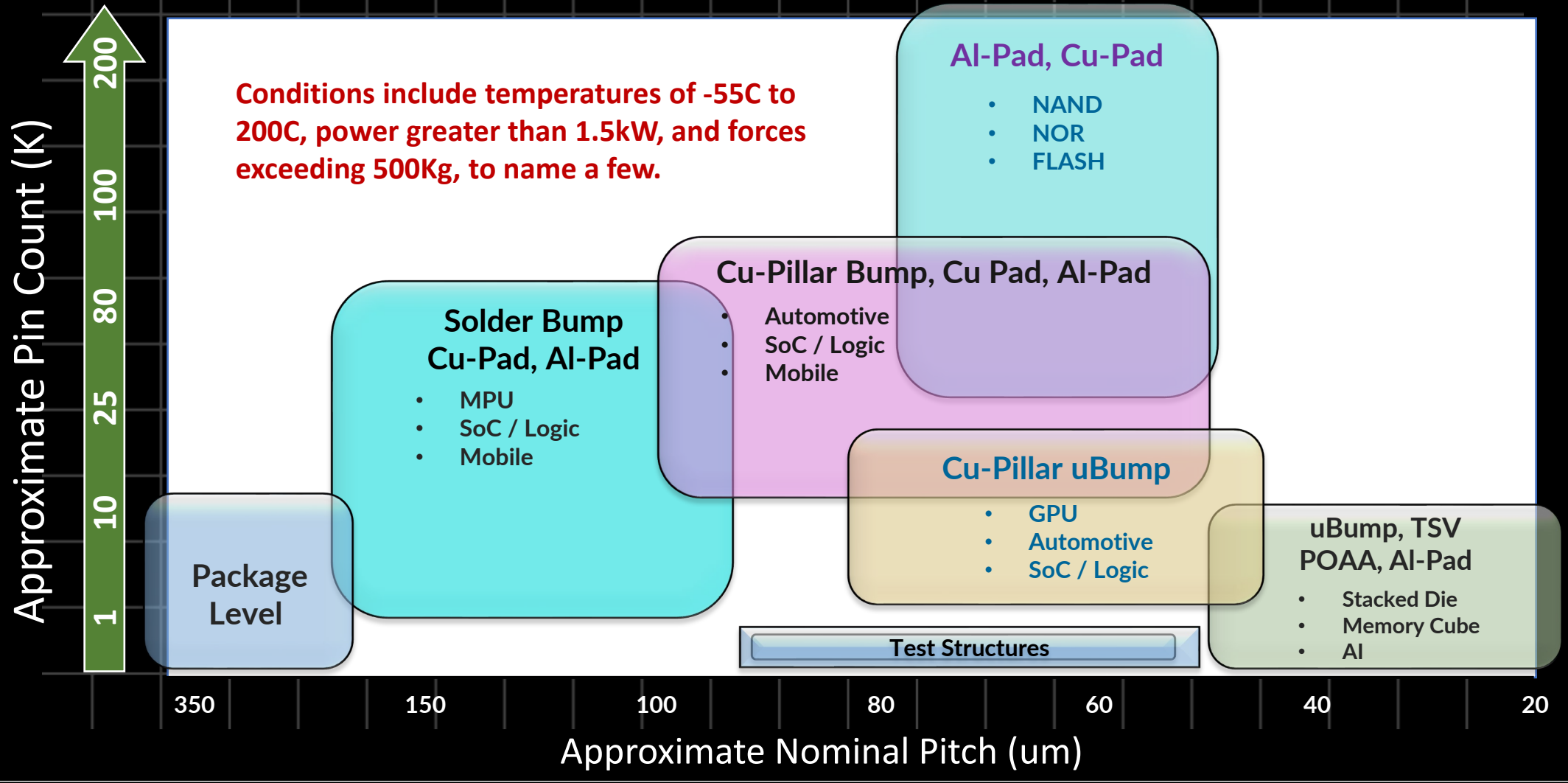


MEMs Micro-cantilevered
For Pads



MEMs Vertical
For Bumps, Pillars, and Pads

No SINGLE Probe Card Type Fits ALL Test Requirements!



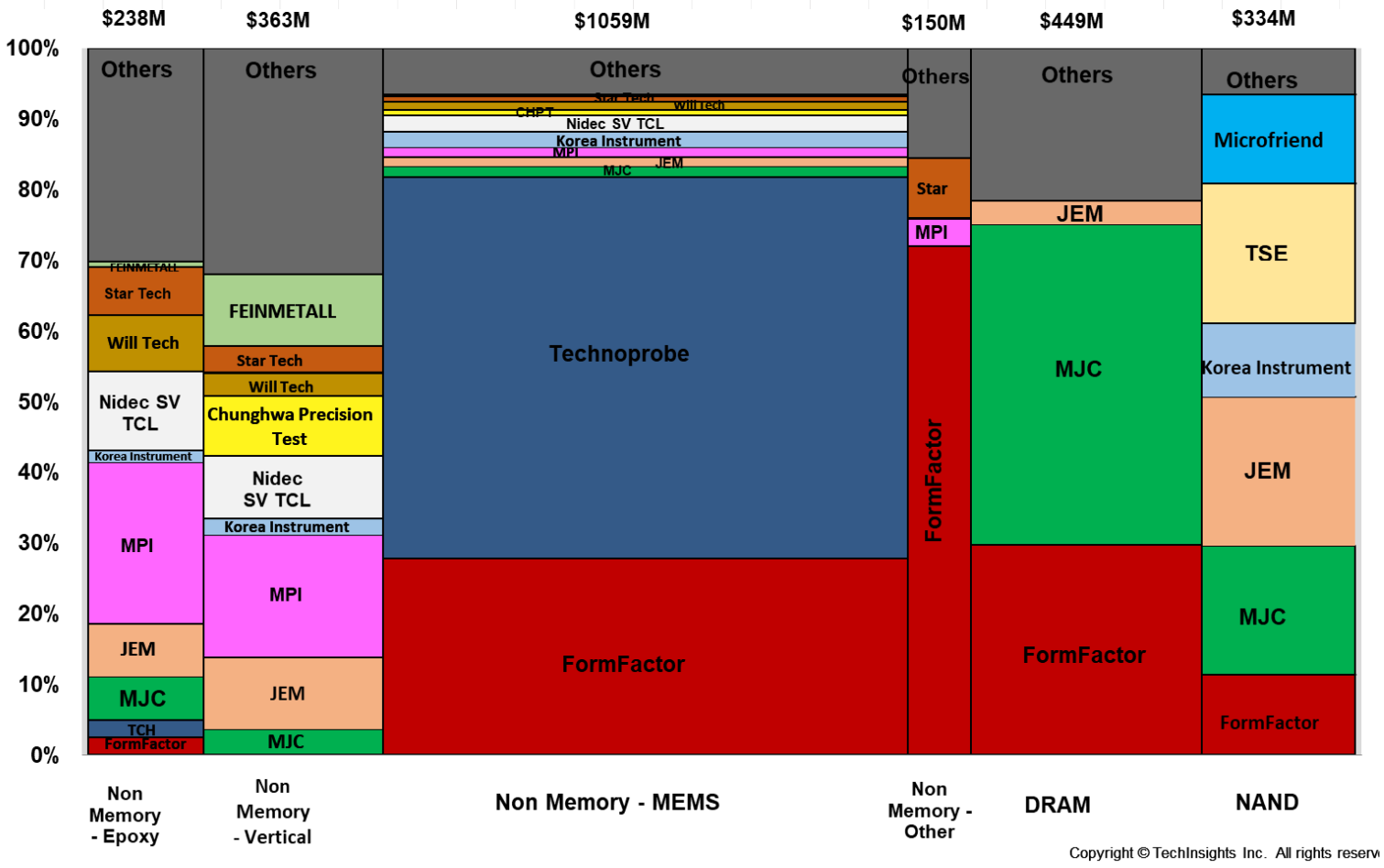
Diverse Probe Card Landscape (2023)

Semiconductor Probe Cards

Sales, $M, Calendar Year

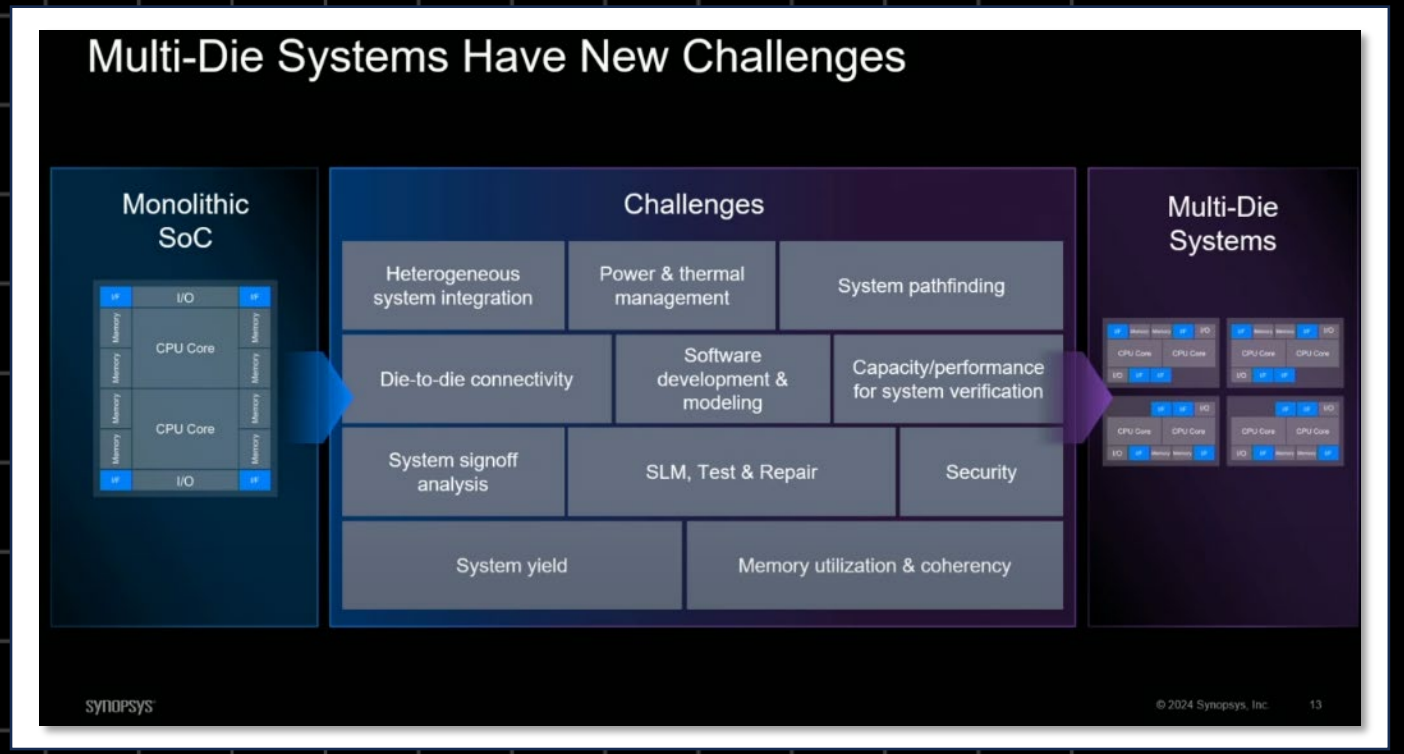
Thanks to TechInsights
- Risto Puhakka
- Panchami Phadke

Rank	Company	Market	% Growth
		2023	YoY
1	FormFactor	497.9	-15.8%
2	Technoprobe	442.5	-23.3%
3	Micronics Japan	259.6	-15.5%
4	MPI Corporation	133.3	-3.7%
5	JEM	116.7	-24.5%
6	Nidec SV Probe	73.2	-13.0%
7	Korea Instrument	65.1	-7.9%
8	Will Technology	46.1	6.2%
9	STAr Technologies	41.1	-19.0%
10	Synergie CAD	40.3	10.8%
	Other	393.7	-13.1%
	Probe Card Sales	2109.3	
	Annual Growth	-17.0%	



Value of Probe Increases for Multi-die Packages

- Continuing with a "monolithic" approach has extremely high development costs.
- Materials and structural innovations have long development cycle times.
- Heterogeneous integration and advanced uses "best-in-class IP" from multiple sources to advance performance at acceptable costs.



Multi-Die Strategies Demand "KGD" (or "Not Bad") Solutions

Source: TSMC Open Innovation Platform® Ecosystem Forum 2019

Critical Probe Data | "KGD" and Multi-Die Packages

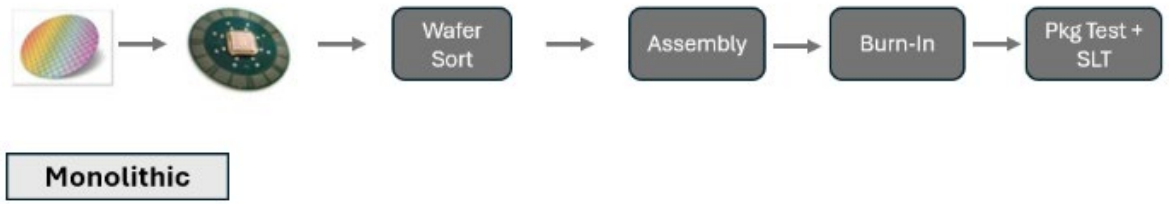
Monolithic

- Basic testing needs to be repeated for each device at each site during wafer sort
  - Connectivity, CRES, Shorts / Opens
  - Added test-time per device
- Traditional wafer test parallelism techniques conflict with testability requirements
  - Test parallelism requires reducing probe counts per die (or higher tester channel count)
  - Reducing probes drive limitations at wafer-test
  - Disaggregated die with tight pitch micro-bumps pose signal integrity challenges
  - High need for identifying KGD at wafer- sort.
- All these trade-offs for cost vs. complexity need to be carefully considered.

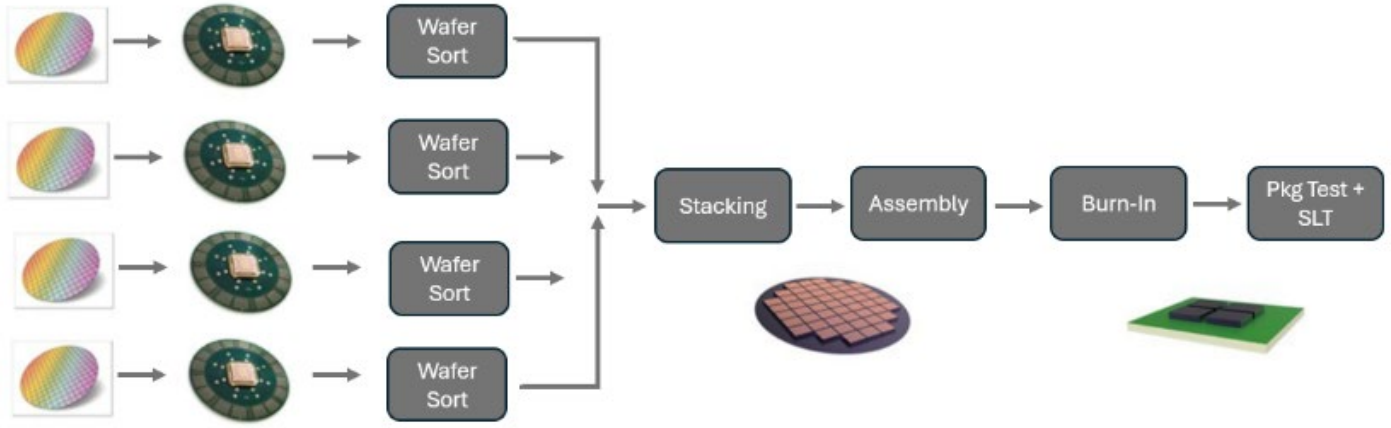
Shift More Test to Probe (Shift to the Left)

Source: S. Ruiwale, P. Tadayon, and G. Iovino, MEPTEC HIT 2022

Critical Probe Data | "KGD" and Multi-Die Packages



Monolithic



Disaggregated

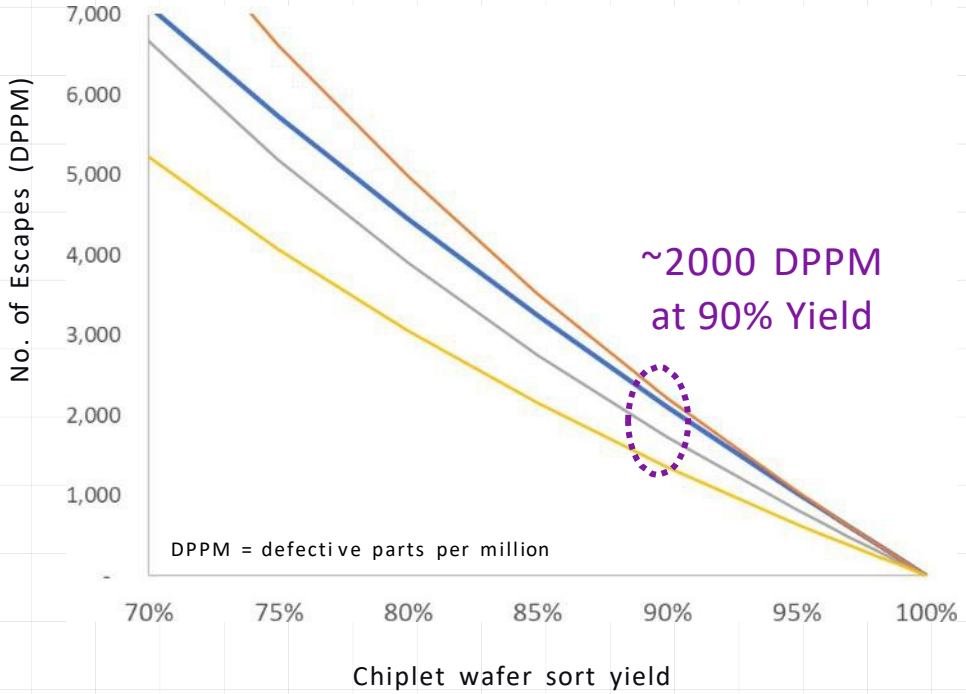
Shift More Test to Probe (Shift to the Left)

- Basic testing needs to be repeated for each device at each site during wafer sort
  - Connectivity, CRES, Shorts / Opens
  - Added test-time per device
- Traditional wafer test parallelism techniques conflict with testability requirements
  - Test parallelism requires reducing probe counts per die (or higher tester channel count)
  - Reducing probes drive limitations at wafer-test
  - Disaggregated die with tight pitch micro-bumps pose signal integrity challenges
  - High need for identifying KGD at wafer- sort.
- All these trade-offs for cost vs. complexity need to be carefully considered.

Source: S. Ruiwale, P. Tadayon, and G. Iovino, MEPTEC HIT 2022

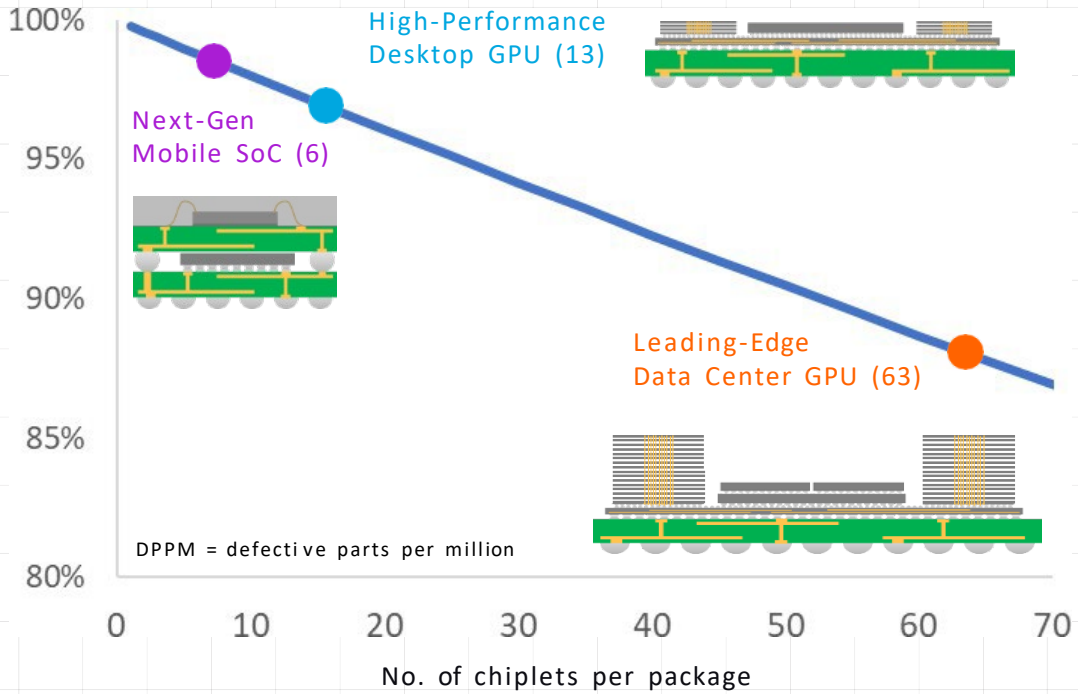
Critical Probe Data | "KGD" and "Not-Bad" Die

Chiplet test escapes from wafer sort at
98% test coverage for various escape models



Number of Escapes Depends on Test Coverage and Yield

Package yield @ **2000 DPPM** average chiplet escape rate



Package Yield Lower With Increased Number of Chiplets

Expensive challenge with increased die count

Source: O. Donzella, SEMICON Europe, 2022

“Shift to the Left” | New Probe Strategies

1. New probing technologies must facilitate cost efficient test of singulated die and stacks of die.
2. Wafer prober, test cell, and devices handlers to support singulated die.
3. Cost effective methods to universally handle numerous die sizes after saw, thin, and bump.
4. Reduce scrapped die due induced defects (saw, thin, bump, etc.) in shared assemblies.

- Significant work underway to allow die to be reassembled in silicon panels that have a rectangular shape as opposed to the round shape of the original silicon wafer.

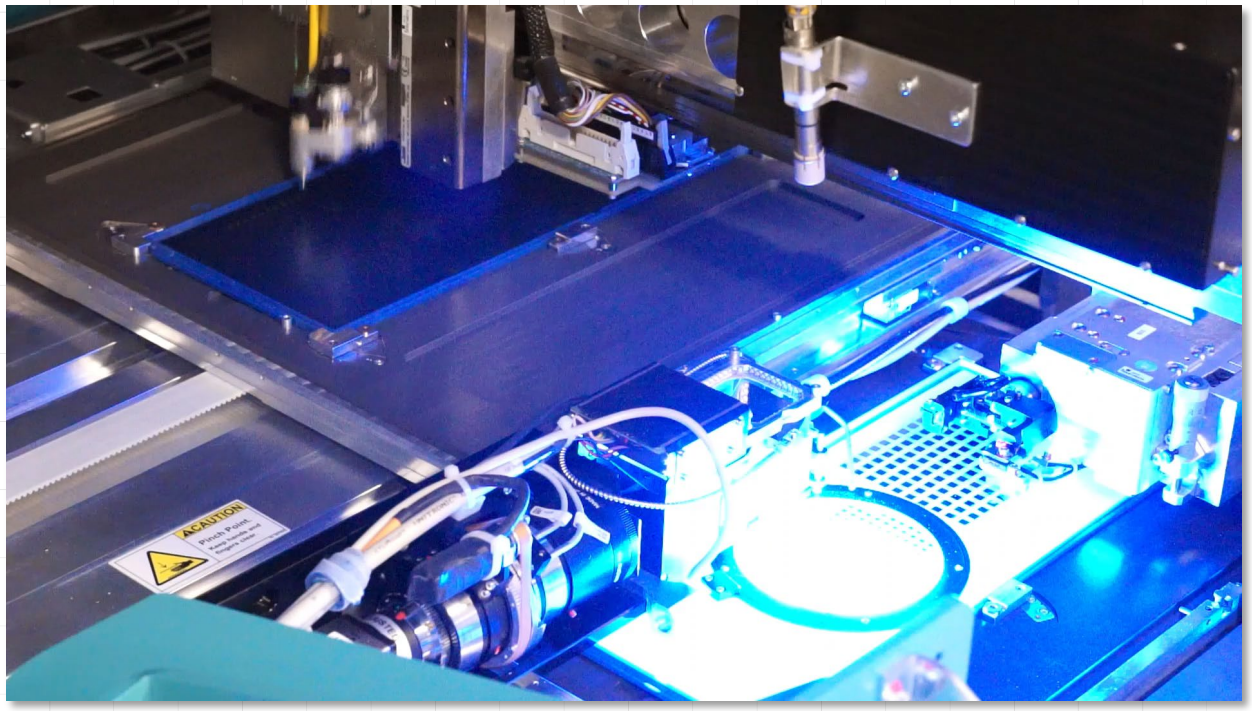
- Universal / Pocketless Tray Formfactor
- Minimal Contact with Devices
- Optimal Holding Force

“Shift to the Left” | New Probe Strategies

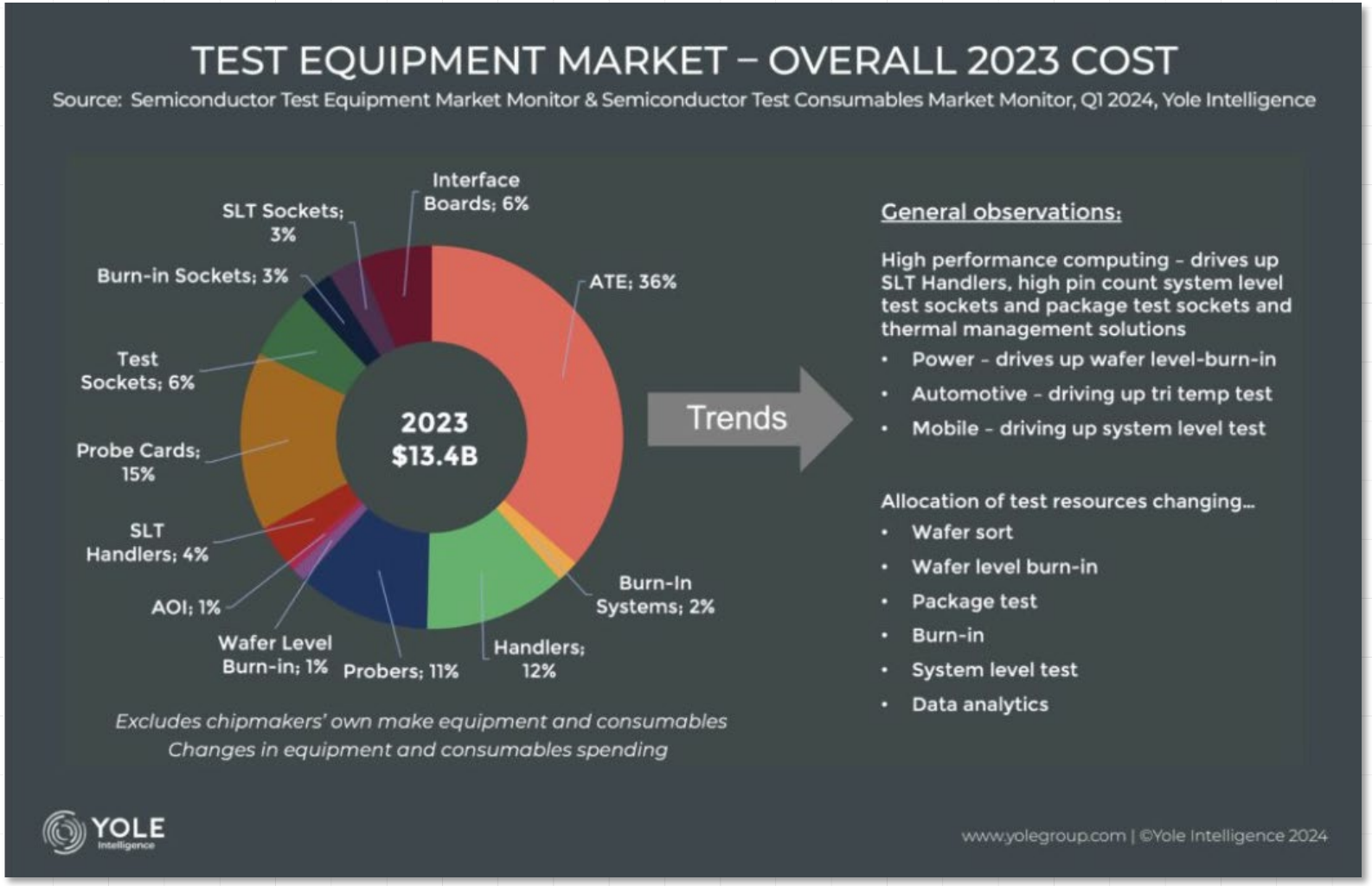
1. New probing technologies must facilitate cost efficient test of singulated die and stacks of die.
2. Wafer prober, test cell, and devices handlers to support singulated die.
3. Cost effective methods to universally handle numerous die sizes after saw, thin, and bump.
4. Reduce scrapped die due induced defects (saw, thin, bump, etc.) in shared assemblies.

- Significant work underway to allow die to be reassembled in silicon panels that have a rectangular shape as opposed to the round shape of the original silicon wafer.

- Universal / Pocketless Tray Formfactor
- Minimal Contact with Devices
- Optimal Holding Force



Increased Cost of Test | Test Equipment Landscape



Outline

- Gel-Pak | Delphon Corporate Snapshot
- Semiconductor Landscape
- Mission of Wafer Test
- Lab to Fab Challenges
- Summary and Takeaways

Lab to Fab

- Device Characterization
- Design Validation
- High Power
- RF-mmW
- Wafer Level Reliability
- Failure Analysis

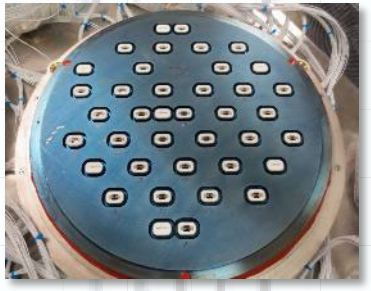
- Data extraction and analysis are crucial from test lab to fab manufacturing.
- Each phase produces vital information for successive phases.
- Insights gained in the lab are critical for efficiency on the production floor.

Engineering Probing

Engineering Labs

Modeling / Characterization

Device Labs
Modeling Labs
Characterization Labs



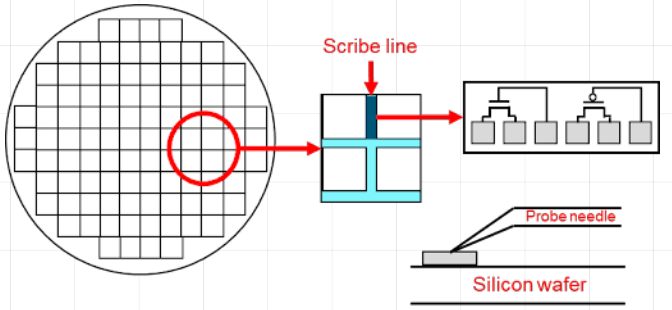
Wafer Level Reliability

Burn-In Labs
Reliability Labs
High Volume Manufacturing

Parametric Test

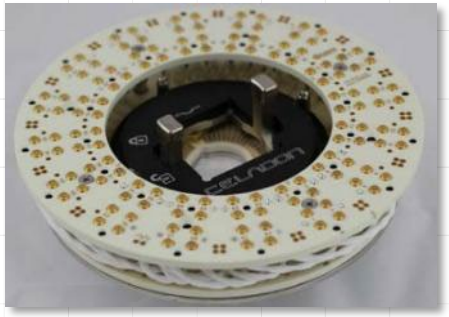
Device Labs
First Silicon Analysis
High Volume Manufacturing

Lab to Fab | Critical Data



- **Critical Data Targets: maximize production yields by identifying potential issues early in the process.**

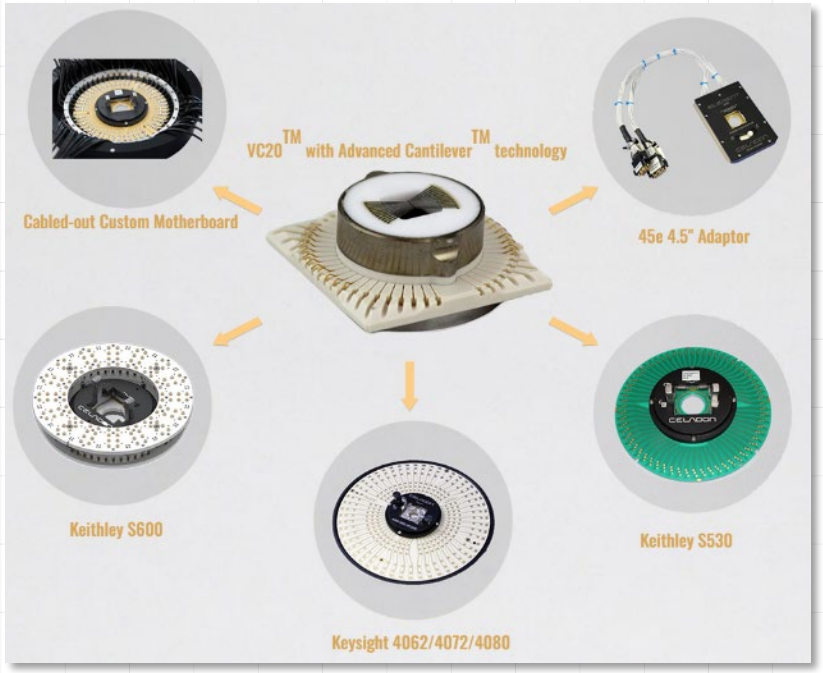
- Parametric Test & Structures
  - Located in the region between adjacent die.
  - Vary within the scribelines and stability of the silicon process.
  - Provides the data to judge whether silicon process is in control.
  - No 1:1 correlations between product die and parametric test results.



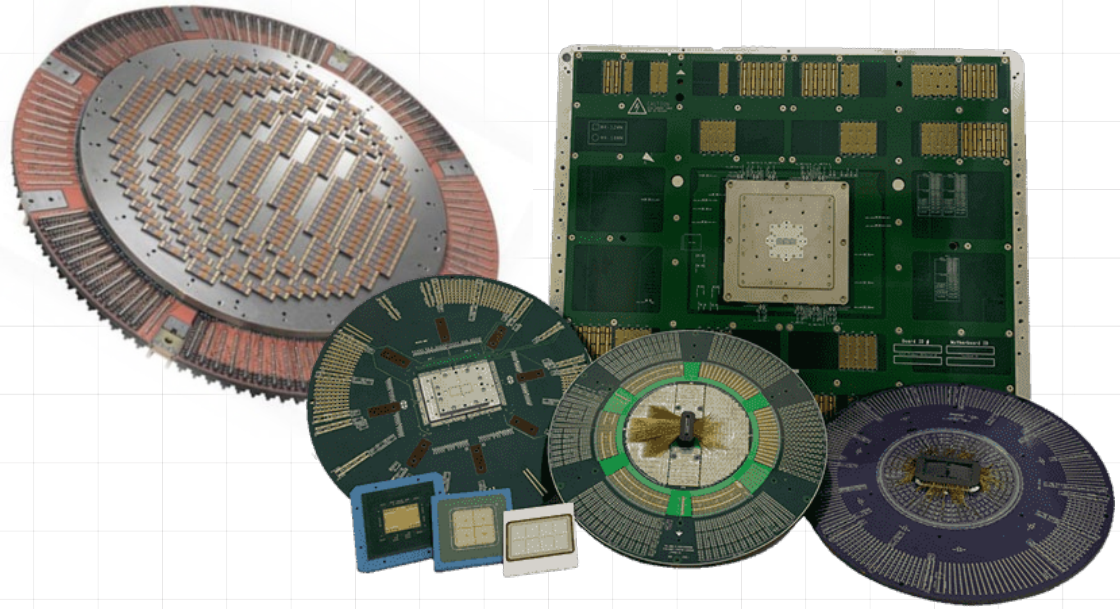
- Basic electrical characteristics on the wafer:
  - Transistor threshold voltage
  - Leakage current
  - Capacitance
  - Resistance
  - Diode Characteristics

- Parametric tests evaluate the wafer fab's process capability of yielding product die and monitor the health of a factory as a function of time and material.

Lab to Fab Challenges | Probe Scaling

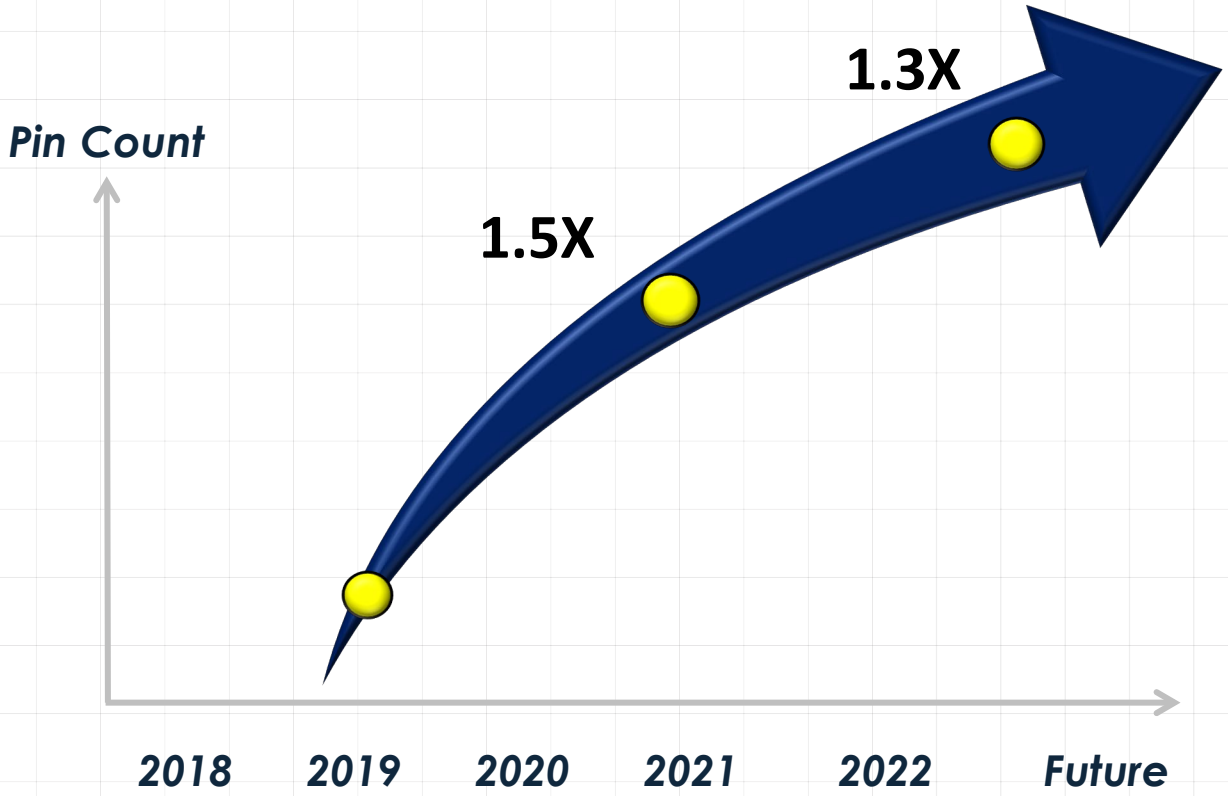


- Parametric: up to 48 channels @ 50um pitch
- Minimum Pad Size: 30um x 30um
- Contact Resistance: <1 ohm
- Temperature: -65C to +200C
- Lifetime performance: +10M TDs

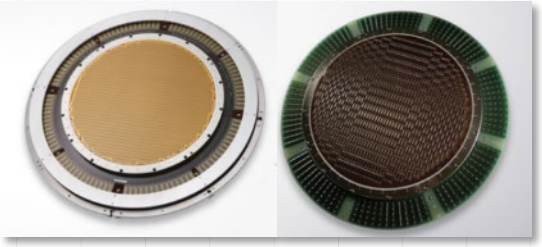


- DRAM: 1-TD, X2000 DUT, >175K probes @ 60um pitch
- Logic: X16 DUT, >80K probes @ 75um pitch
- Temperature: -40C to 175C
- Lifetime performance: 100K to 2M TDs

Probe Challenges | High Pin Counts

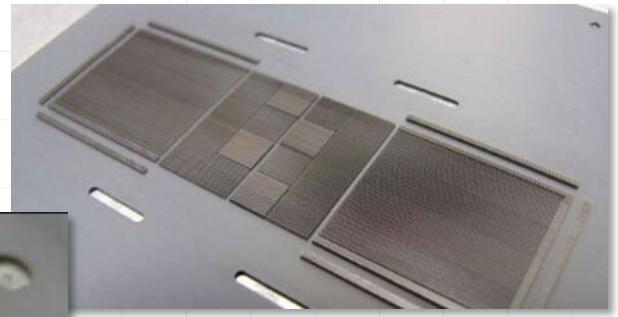


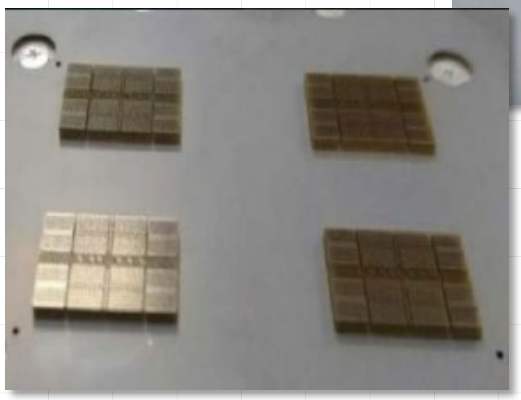
Memory
150K to 200K Pins
500 to 700Kg



Source: MJC Website

Non-Memory
80K to 120K Pins
175 to 200Kg

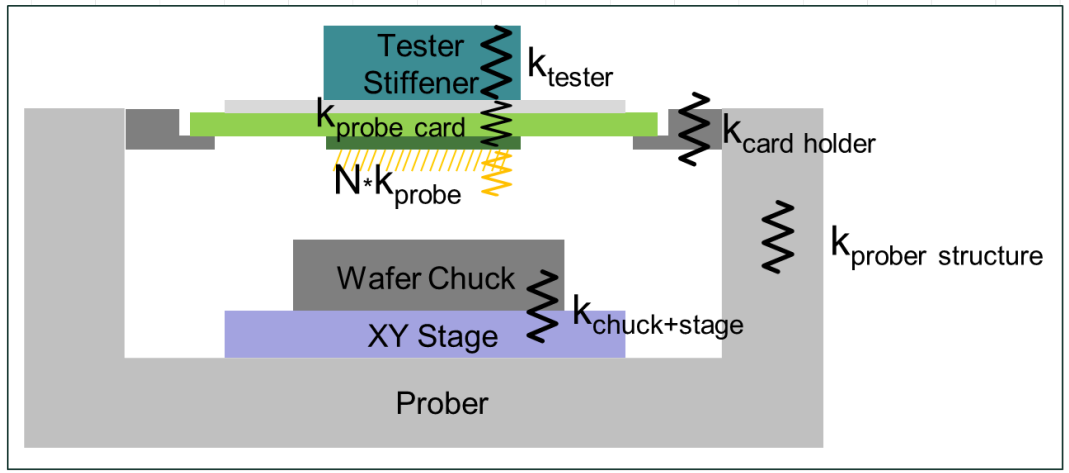




Source: K. Martin, SWTest 2023

Source: E. Bertarelli , SWTest 2020

Probe Challenges | AOT vs. POT

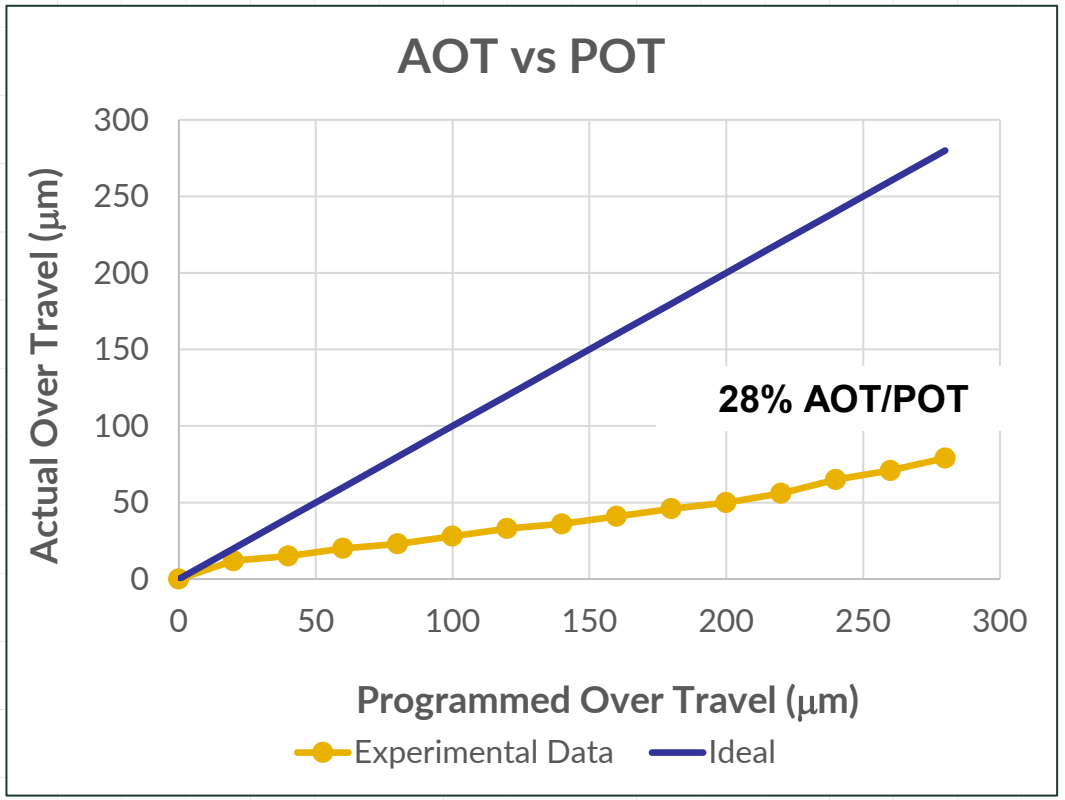


The system consists of a group of springs in series:

$$\frac{1}{k_{system}} = \frac{1}{k_{probe\ card}} + \frac{1}{N * k_{probes}} + \frac{1}{k_{card\ holder}} + \frac{1}{k_{prober\ structure}} + \frac{1}{k_{chuck+stage}} + \frac{1}{k_{tester}}$$

where N = number of probes

Actual compression of the probes is less than programmed due to non-infinite system stiffness.

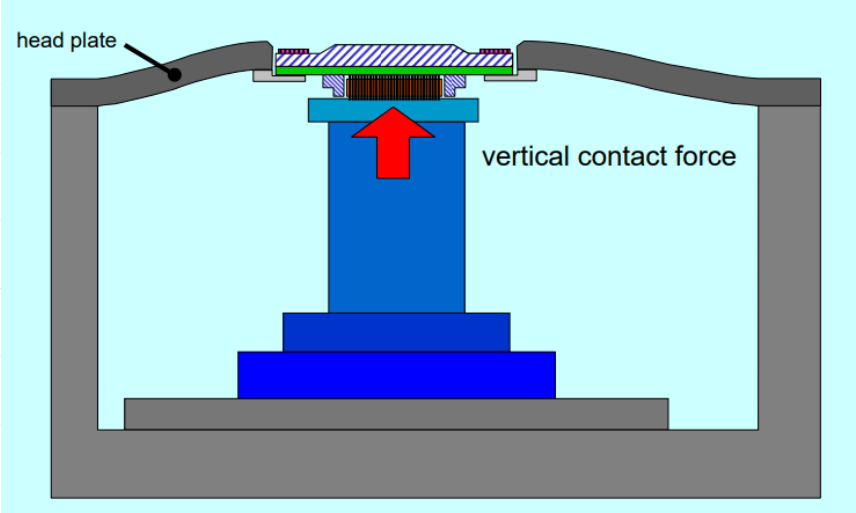


Source: T. Berry. K. Breinlinger, R. Rincon, SWTest, 2012

Source: K. Martin, SWTest 2023

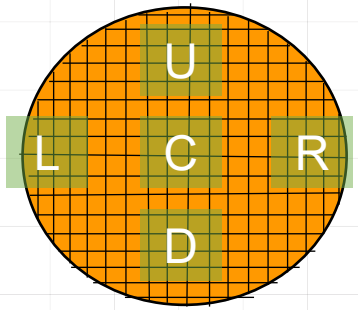
Probe Challenges | Contact Force

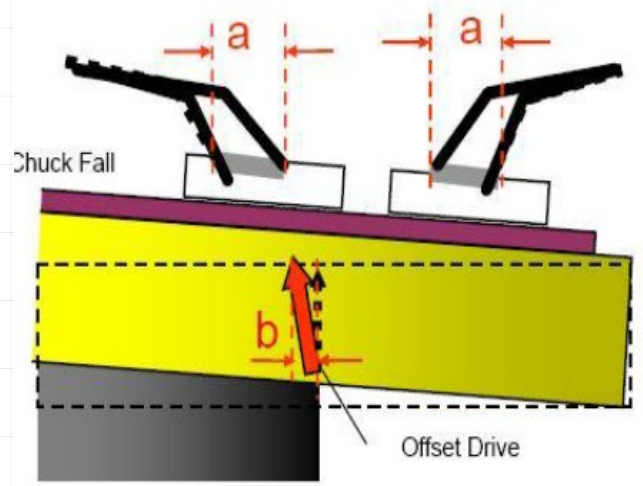
- **Probers need high force wafer chuck options pushing the limits to more than 700 kg.**
  - 200K probes at 2.5 gf each
  - **> 500 kg total force!**
- **High pin count probe card, the significant decrease in AOT is the system deformation.**



Source: G. Boehm, SWTest, 2006

- **Probers need minimal chuck deflection during offset high force loading condition**
  - 80k probes at 2.5 gf each
  - **> 200 kg off-set total force!**
- **Non-uniform AOT is observed with offset loading using high pin count arrays.**





Source: O. Lee, SWTest Asia 2022; K. Tang, SWTest, 2023

Probe Challenges | Probers, Interfaces, and Testers

Accretech AP3000 Prober

Accretech AltaProv Modular Prober

Advantest DUT Scale Duo Tester

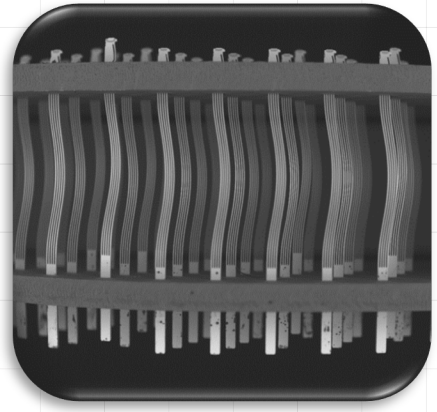
TEL Prexa Prober

TEL Cellcia Modular Prober

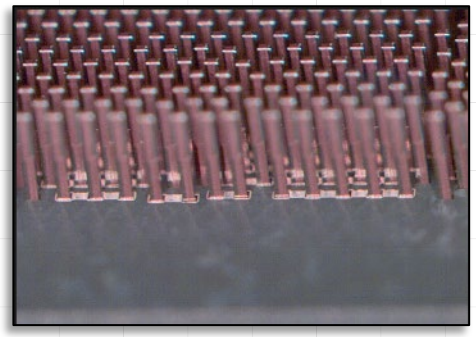
Teradyne UltraFLEXplus Tester

Probe Challenges | CCC

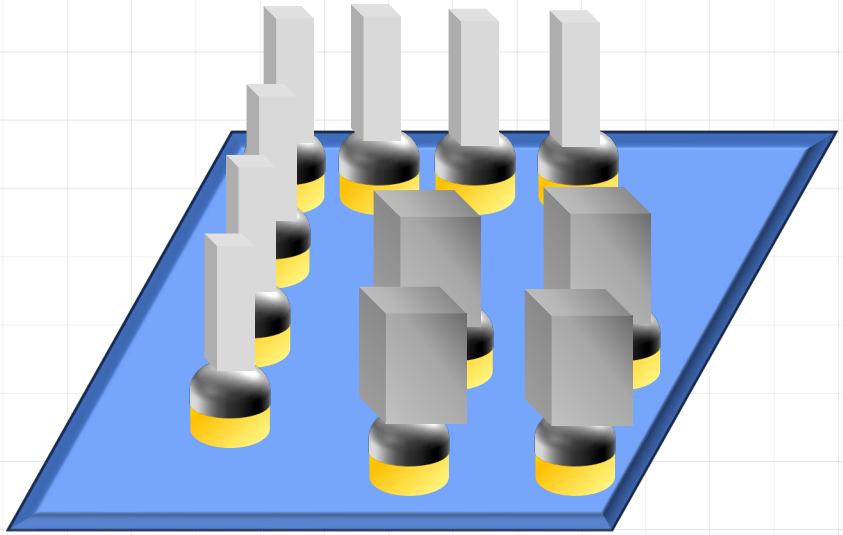
Next Generation Metallurgies



Metallized Guide Plates

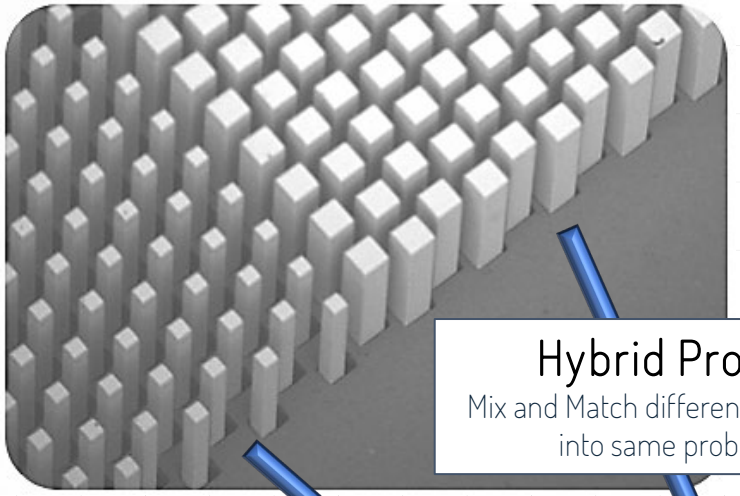


I/O and High Speed
Fine Pitch < 100um

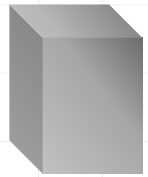


Power and GND
Wide Pitch > 100um

Higher CCC
(> 1,000A at 1V)



Hybrid Probing
Mix and Match different probe types into same probecard

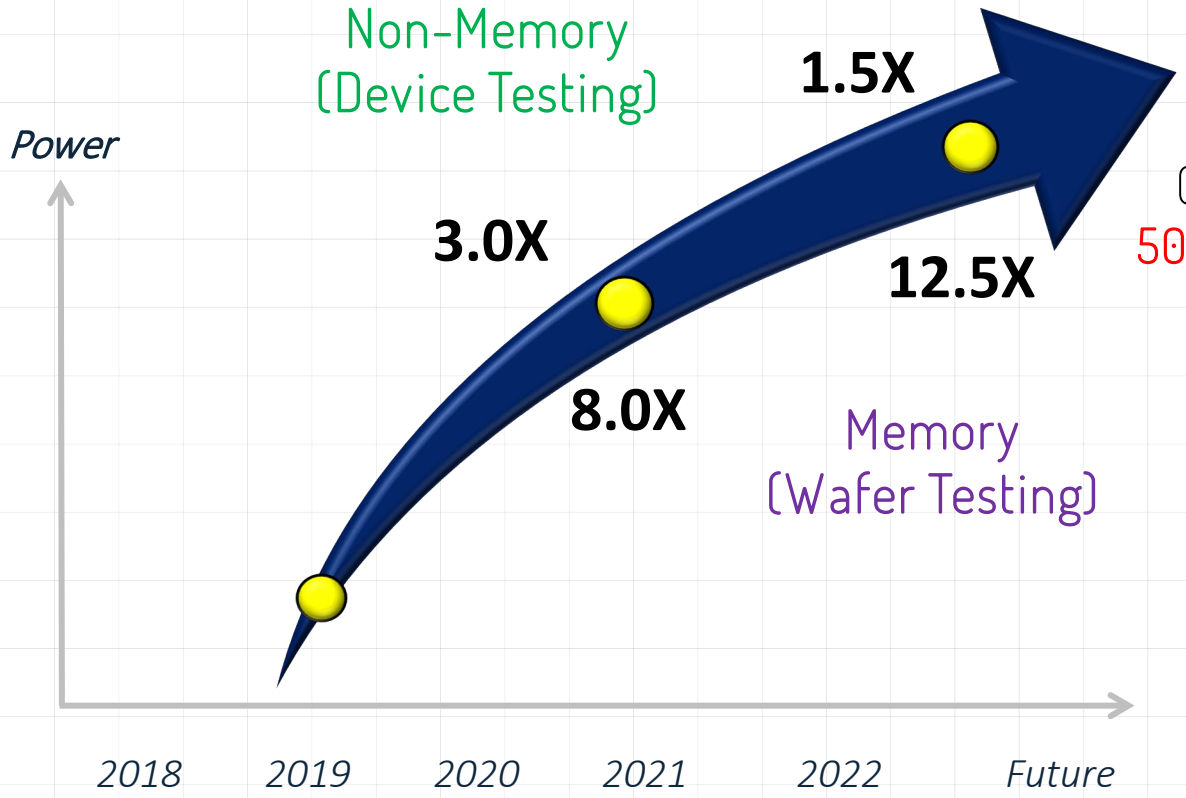
Probe type		
Pitch(um)	< 100	> 100
CCC	1.0X	***1.39X***

Source: D. Raschko , SWTest 2023; H. Nadir SWTest Asia 2023

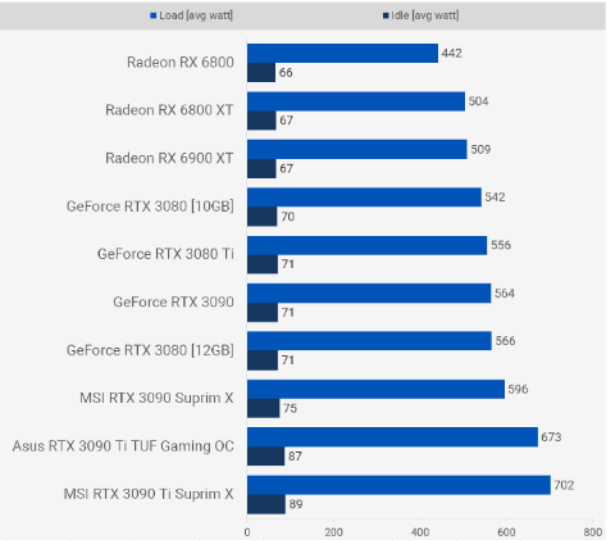
Source: O. Lee, SWTest Asia 2022; K. Tang, SWTest, 2023

Probe Challenges | Power

High Power & Current
HPC and GPU
1.5kW per Device

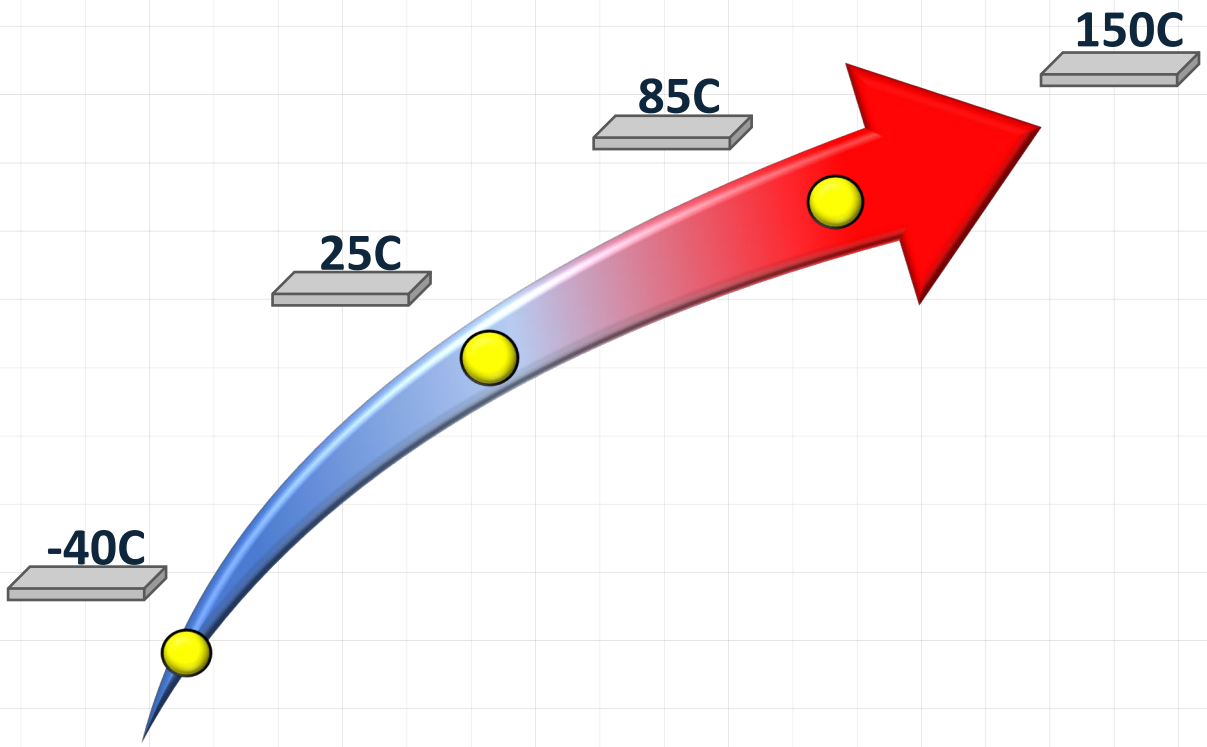


One-Touch Contact
500 to 600W per Wafer



https://www.techspot.com/article/2540-rise-of-power/; IEEE HiR Roadmap 2023 - Chapter 17

Probe Challenges | Temperature



Demanding Automotive Reliability Requirements

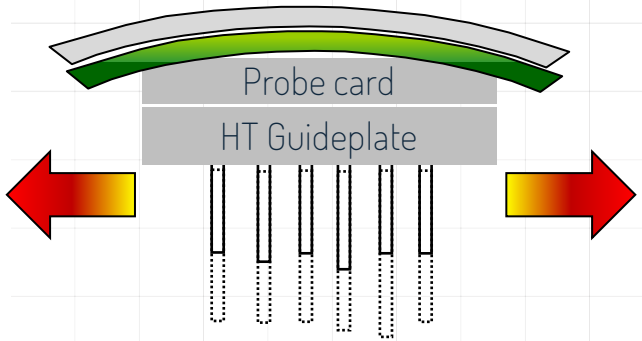
AEC Q-100 Grade	Temperature	Segment	
0	-40C to +150C	Powertrain	
1	-40C to +125C	Body, ADAS	
2	-40C to +105C	Chassis, ADAS, Safety, Powertrain	
3	-40C to +85C	ADAS, Sensors, Infotainment	

Source: Automotive Electronics Council : AEC-Q100

Probe Challenges | CTE Mismatch

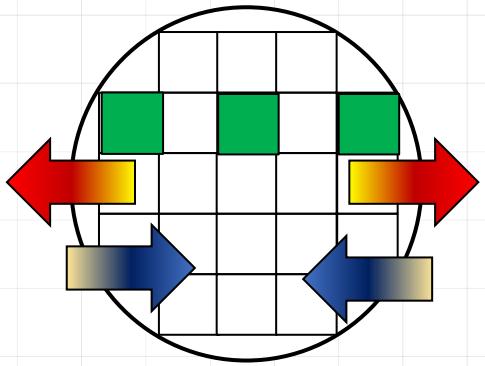
- **CTE (Coefficient of Thermal Expansion) mismatches cause deformations and affect probe-to-pad and probe-to-bump misalignment.**

- **Preheat and soak to assure for thermal stability.**

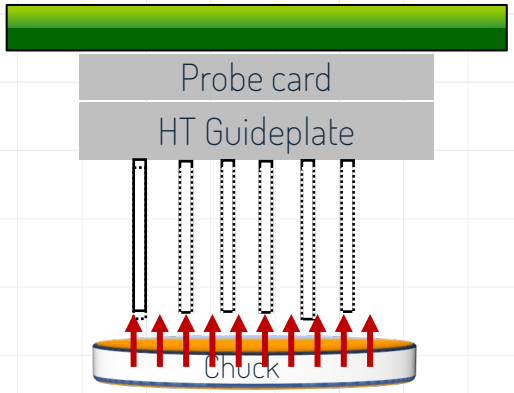


- Probe Expansion
- Probe Card ST Flex
- MLO Bowing
- Stiffener Flex

Heat



- Wafer Expansion
- Wafer Contraction
- Thermal Variation

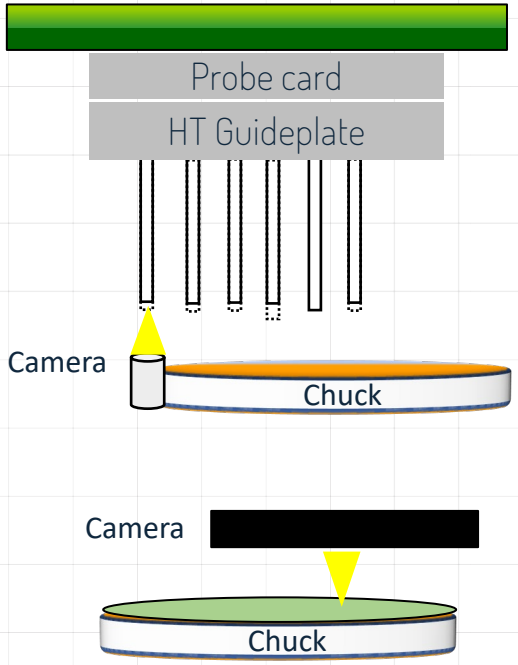


Heat

Preheat

(ex. Contact Preheat)

Soak to Stabilize



Stable Alignment

(Needle & Wafer alignment)

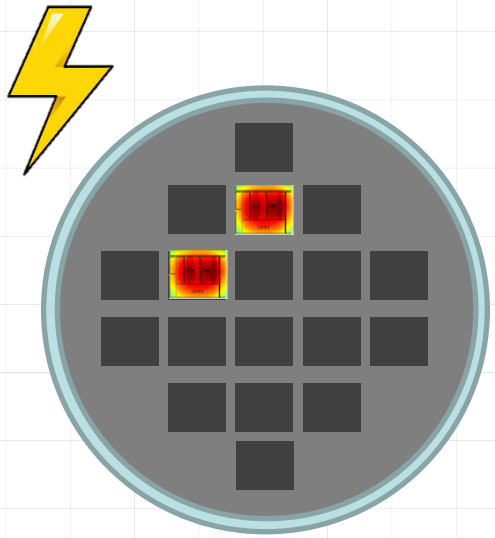
Source: Usai, S. and Barterlli, S., SWTest 2021; O. Lee, SWTest Asia 2022; K. Tang, SWTest, 2023

Probe Challenges | Localized Heating

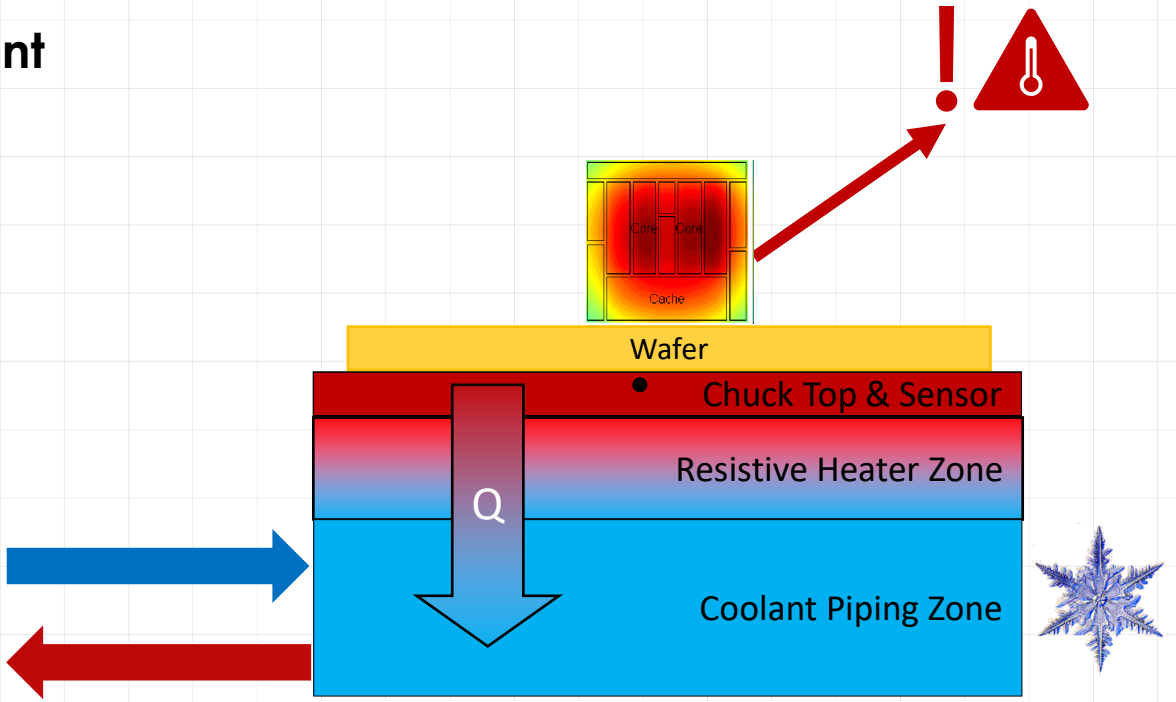
- High current and high-power create localized die heating.
- Heat dissipation and thermal management

High Current (>10A)

High Power (>600W)



Concentrated Heat Application
Automotive Device Testing



$Q_{CPZ} = Q_{RHZ} \rightarrow Q_{CPZ} = \downarrow Q_{RH} + Q_W$

$Q_{Static} = Q_{Test}$

Source: O. Lee, SWTest Asia 2022; K. Tang, SWTest, 2023; L. Huston, SWTest 2023

Probe Challenges | Contact & Lifetime (Cleaning)

- **Probes touch the DUT, but the Current Might NOT Flow !**
- **Probe cleaning is a "dirty business" and critical for controlling contact.**
- **Cleaning can consume more 95% of a probe card lifetime.**

METALLIC CONTACT

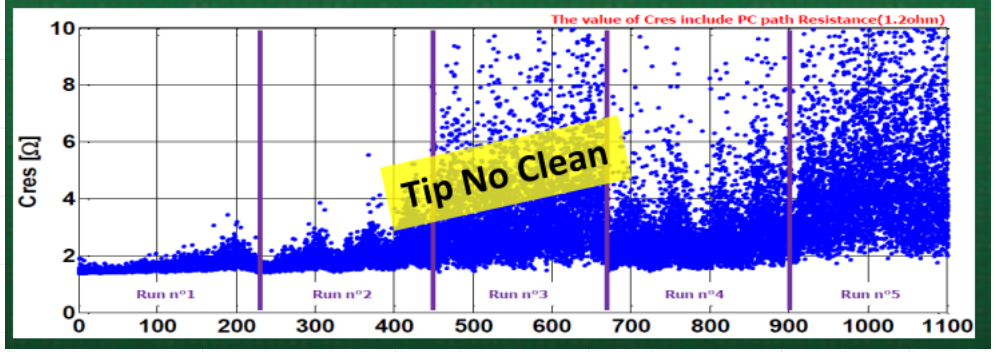
Film Resistance

$$C_{RES} = \frac{(\rho_{probe} + \rho_{pad})}{4}\sqrt{\frac{\pi H}{P}} + \frac{\sigma_{film} H}{P}$$

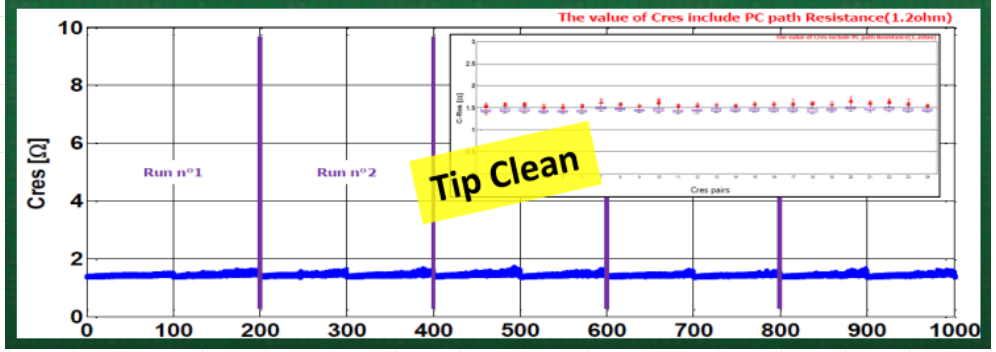
- ρ_{pad}, ρ_{probe}, σ_{film} = resistivity values
- H = hardness of the pads, bumps, pillars, etc.
- P = contact pressure applied by probe

Implement efficient cleaning
to ensure reliable electrical contact.

LOW FIRST PASS YIELD

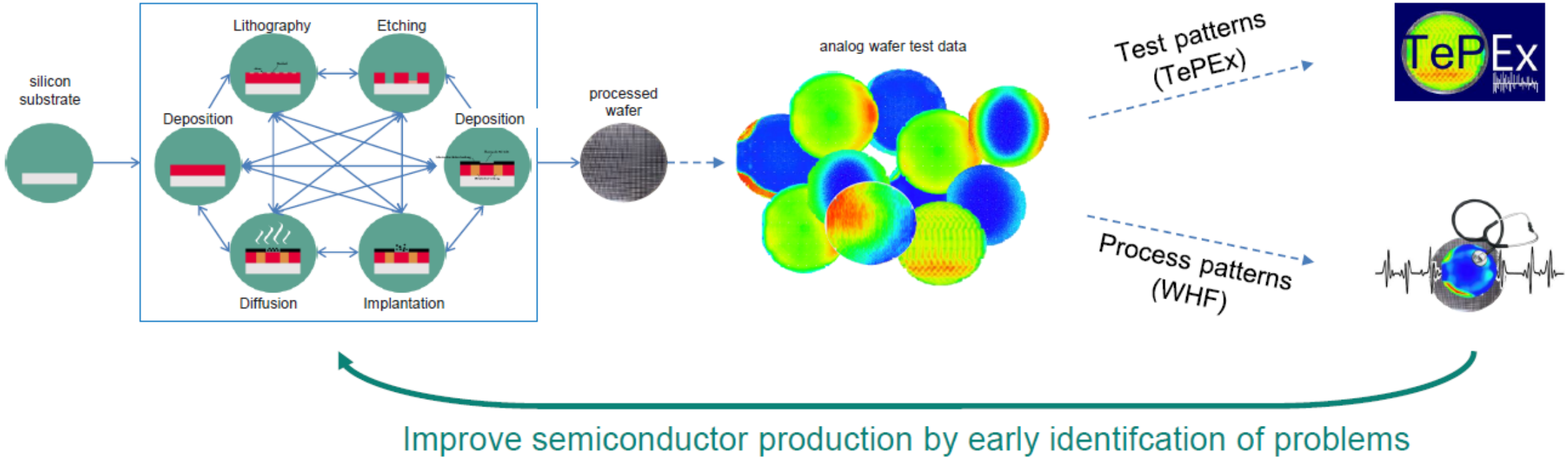


HIGH FIRST PASS YIELD



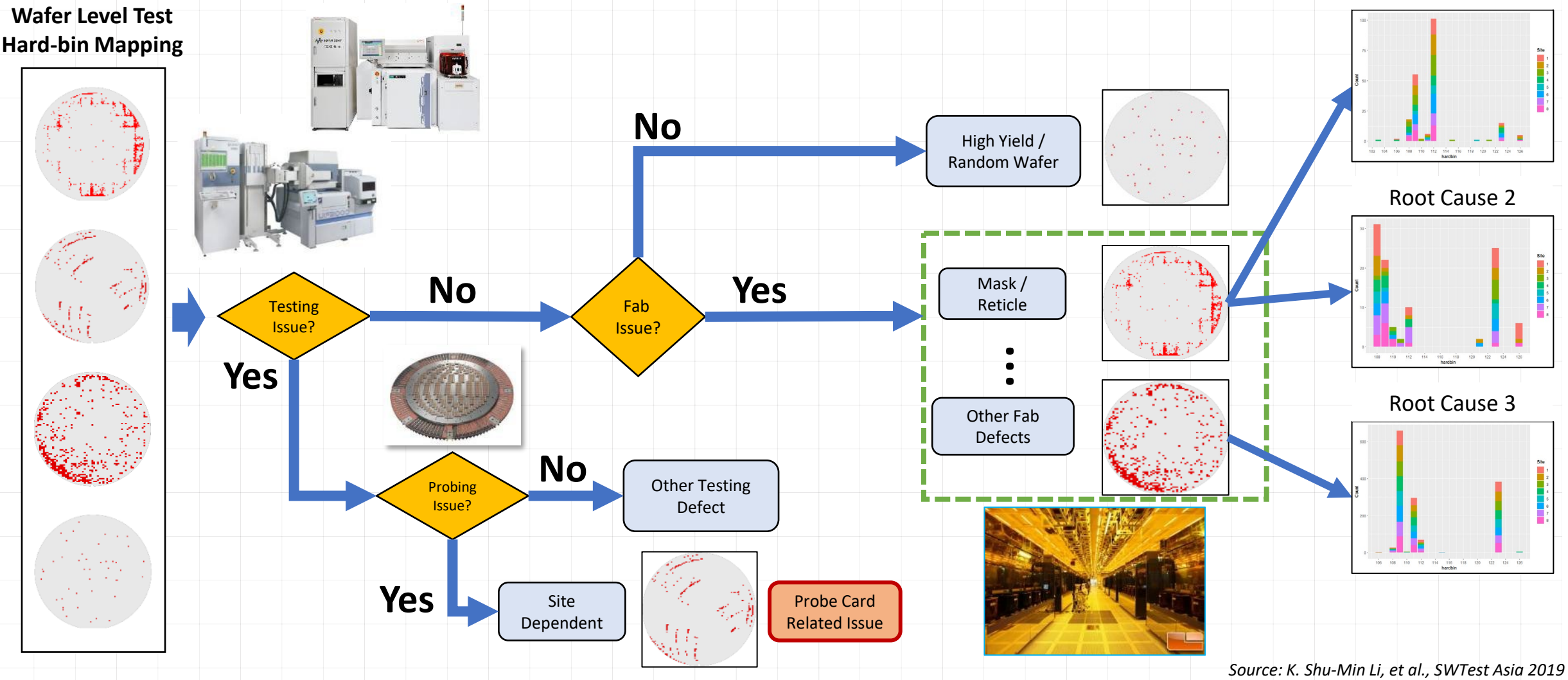
Source: R. Vallauri, D. Perego, M. Prea, J. Kim, and J. Yun, SWTest 2017

Critical Probe Data | AI Analysis for FAB



Source: M. Scheiber, ISTest Workshop 2024

Critical Probe Data | AI Process Feedback



Source: K. Shu-Min Li, et al., SWTest Asia 2019

Outline

- Gel-Pak | Delphon Corporate Snapshot
- Semiconductor Landscape
- Mission of Wafer Test
- Lab to Fab Challenges
- Summary and Takeaways

Summary and Takeaways

- 2nd Tier IDMs, foundries, and OSATs must rely more heavily on test thoroughness going from the Lab to the Fab .
- Significant challenges are emerging that require technical partnerships to economically address the demands of increased test coverage, increased complexity and data quality.
- Wafer probe must not become a limiter for new technologies and multi-supplier, collaborative innovation is clearly necessary to enable cost-effective, optimized strategies.

Where to Learn About Probe Challenges? | SWTest Conferences

SWTEST

SWTEST ASIA

40 Combined Years of Probe and Wafer Test Technology

12,000+ Attendees from 60+ Countries

1,100+ Technical Podium and Poster Presentations

Repeat Multinational Sponsors and Industry Exhibitors

SWTEST
PROBE TODAY, FOR TOMORROW
2025 Conference and Expo

SWTest 2025
San Diego

June 2 to 4, 2025
Omni La Costa, California

SWTEST ASIA
PROBE TODAY, FOR TOMORROW
2025 Conference and Expo

SWTest Asia 2025
Fukuoka

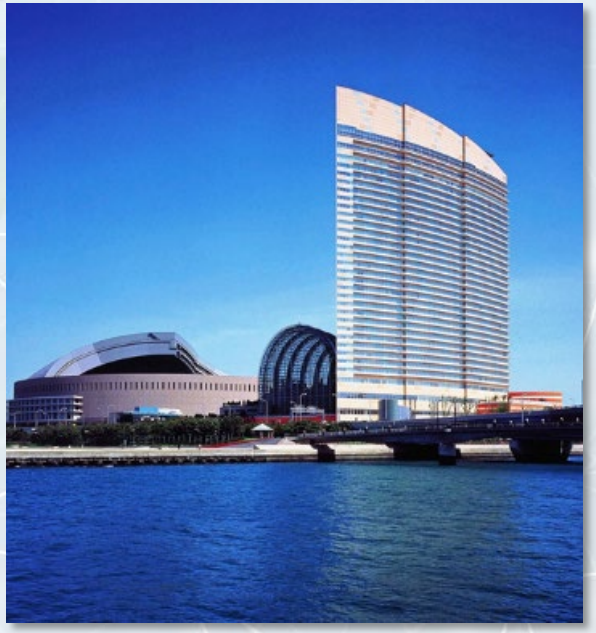
November 20 to 22, 2025
Hilton Sea Hawk, Fukuoka, Japan

SWTest Asia 2025 | Fukuoka, Japan

- **Schedule：November 20 - 22, 2025**
- **Location：Hilton Fukuoka Sea Hawk**

- **Conference Day 1 (Nov. 20, 2025)**
  - Opening and Visionary Keynote
  - Podium Sessions & Poster Sessions
  - Key Supplier Expo
  - Platinum Sponsor Tech-Showcase
  - Networking Event in Expo Hall
- **Conference Day 2 (Nov. 21, 2025)**
  - Opening
  - Podium Sessions & Poster Sessions
  - Key Supplier Expo
  - Platinum Sponsor Tech-Showcase
  - Networking Event
- **Charity Golf Tournament and Networking Day 3 (Nov. 22, 2025)**
  - Benefit Golf Tournament to support student participation.

SWTEST ASIA
PROBE TODAY, FOR TOMORROW
2025 Conference and Expo



THE CLASSIC GOLF CLUB

Achnowledgements

- Victoria Tran, PhD - R&D Director at Delphon
- Rajiv Varma - CTO at Delphon
- Joseph Montano - CEO at Delphon

Questions ?

DELPHON
Merging Innovative Technologies

DELPHON

Merging Innovative Technologies

Increasing the Role of Probe from Lab to Fab: The Mission of Critical Data

Jerry Broz, PhD

VP of Business Development & Strategic Marketing, Delphon Industries, LLC.

General Chair of SWTest Conferences

Gel-Pak®

Protecting the World's Valuable Devices