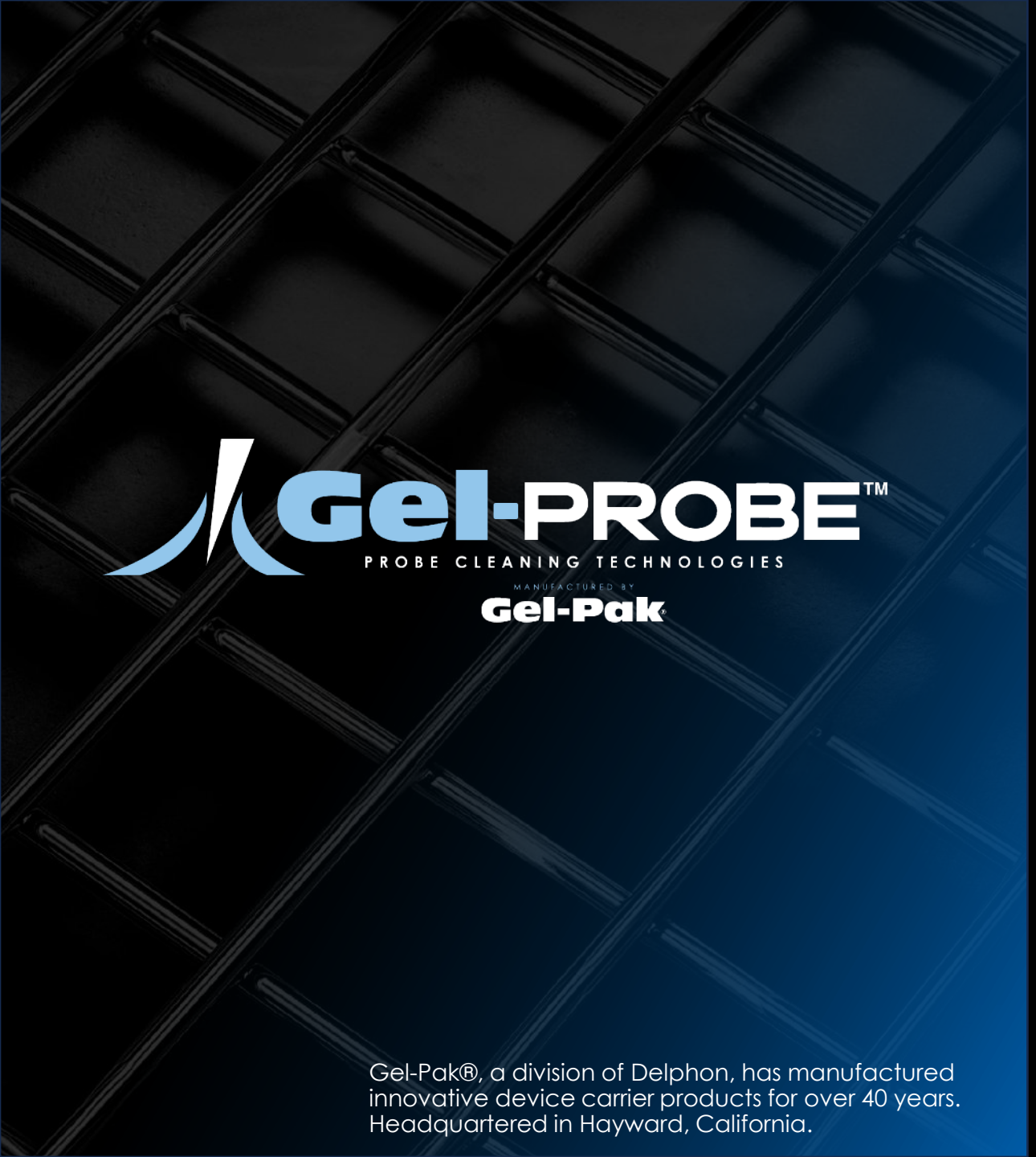


Gel-Pak®, a division of Delphon, has manufactured innovative device carrier products for over 40 years. Headquartered in Hayward, California.

Gel-Probe Cleaning Technologies

Maximize Yield and Reduce Cost of Test

Jerry Broz, PhD

VP, Strategic Marketing and Business Development

Victoria Tran, PhD

Director of Research and Development

Overview & Agenda

- Gel-Pak | Delphon Snapshot
- Probing is a “Contact” Sport
- Probe Cleaning is Mandatory | Maximize OEE
- Gel-Probe for Efficient Probe Cleaning
- Customer Case Studies | Qualifications
- Summary & Takeaways

Gel-Pak | Delphon | At-A-Glance

Gel-Pak®
Protecting the World's Valuable Devices

Device Protection and Elastomer Film Solutions

TOUCHMARK
MEDICAL DEVICE PAD PRINTING

Specialty Printing and Coating Solutions

UltraTape
Adhesive Tapes and Labels for Critical Environments

Tapes and Labels for Cleanroom Environments

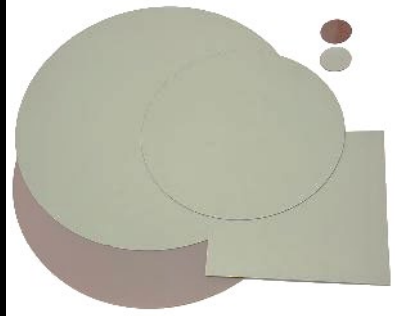
Merging Innovative Technologies

DELPHON

- Delphon Industries develops and delivers highly engineered materials for the semiconductor, medical, photonics, and electronic industries.
- High volume, ISO 9001:2015 certified facilities are headquartered in Hayward, CA with operations in Wilsonville, OR, and Johor, Malaysia.
- With 90,000 sq. ft. and several ISO Class 7 cleanrooms, Delphon Divisions have been producing innovative products since 1980.
- Over 1,000 global customers, ranging from Fortune 500 companies to startups to universities labs rely on Delphon expertise and innovation.
- Trusted by numerous industries to handle, transport, or process small, high value devices without risk of damage.

Gel-Pak Innovations that Drive OEE

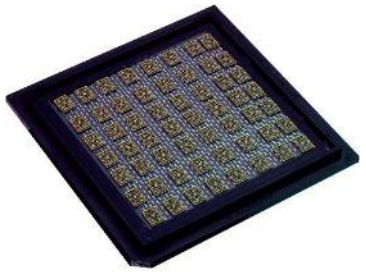
ELASTOMER PROBE CARD CLEANING FILMS



Gel-Probe Card Cleaning

- Custom coating of highly engineered elastomer films for semiconductor applications.
- Customizable probecard cleaning wafer and cleaning sheet applications.

SMALL DIE SHIPPING & HANDLING



Vacuum Release Carriers

- Automated pick & place applications for bare die and devices ranging from <250 micron to 75mm in size.
- Handling small components or large assembled modules.
- Suitable for transport and handling MEMs Probes

DIE WAFER & PANEL SHIPPING & HANDLING

Large Substrate Vacuum Release Carriers™

- Shipping and handling full or partial wafers, panels, and OTHER substrates from 75mm to 450mm.
- Suitable for KGD, singulated die, and film frame loaded devices.

UNIVERSAL & POCKETLESS CARRIERS

Textured Device Carrier Products

- Pocketless \carriers and transport products for KGD and other devices
- Universal Fixture for device handling in-process, singulated die testing, and shipping.

Overview & Agenda

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Probing is a “Contact Sport”!

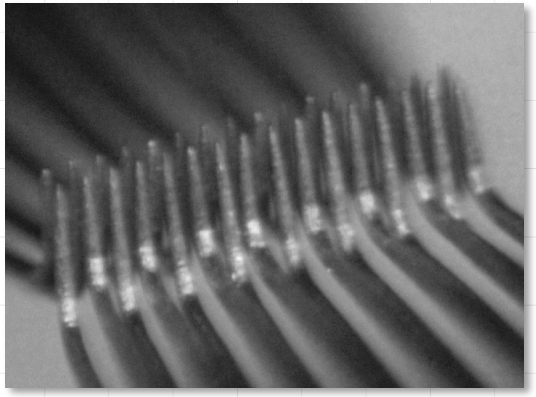
Three key components of basically any wafer-test cell:

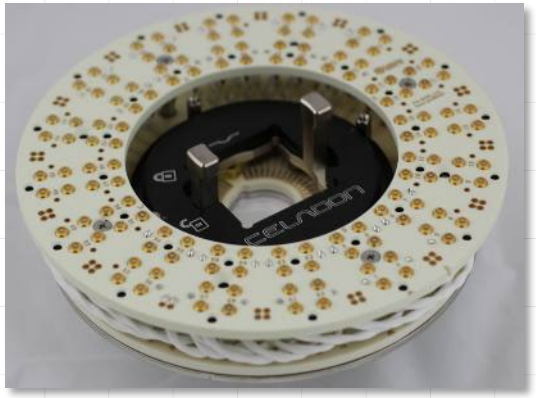
1. **ATE**: Instruments & power supplies that stimulate and interrogate the DUT(s).
2. **Prober**: device wafer handling, positioning, thermal environment, and probe cleaning.
3. **Probe card**: Device-specific interface that provides the electromechanical DUT-to-ATE contact.

https://www.keysight.com/us/en/product/N9100A/4080-series-parametric-test-systems.html

Probes Make the “Contact”!

- Physical contact by small diameter probes onto the I/Os of individual DUTs.
- Production probe-cards are specialized for every application.
- Data integrity is critical during parametric testing since Pass / fail criteria are utilized for the ENTIRE wafer.
- Parametric test with low leakage, fast settling times, low cross-talk, guarded traces, temperatures from -55C to 200C.





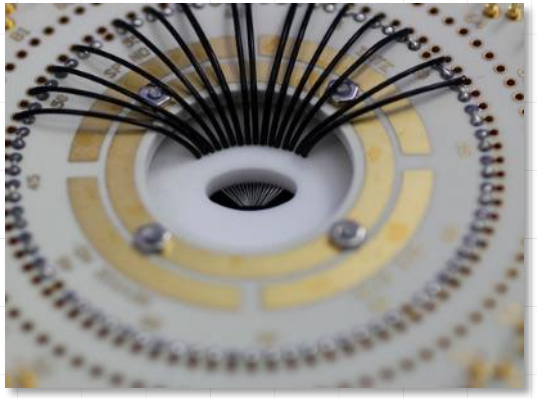
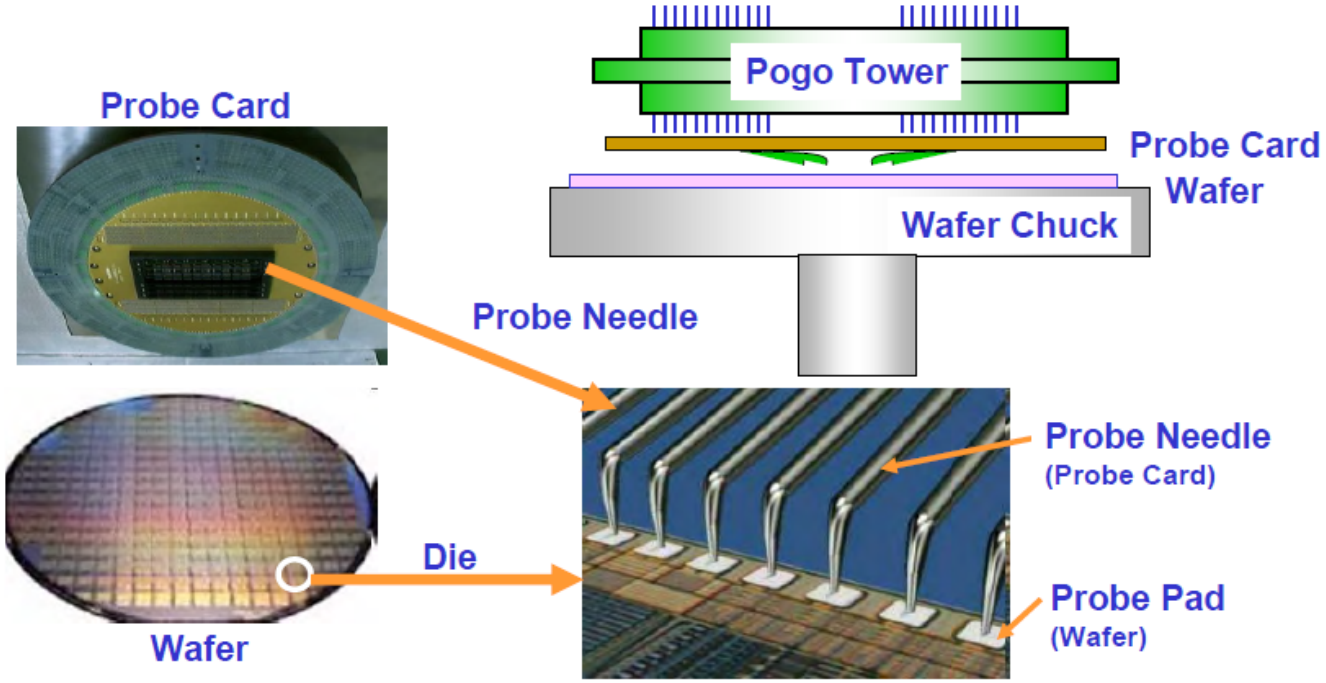


Image Sources: R. Kaiser, et. al, SWTest 2021; Celadon VC20 ELEMENT SERIES

1st Function of Prober = Probe to Pad Alignment

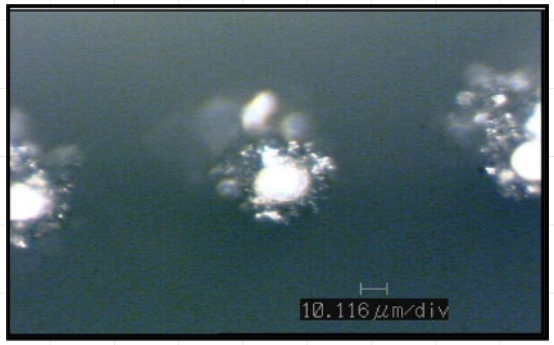
- Precise positioning of wafer in XYZ and indexing under all conditions.
- Aligning the probe tips onto specific test pads on each die or test structure using automated pattern recognition optics.
- Performing all operations with minimal manual intervention, including wafer loading, positioning, and probe card alignment.



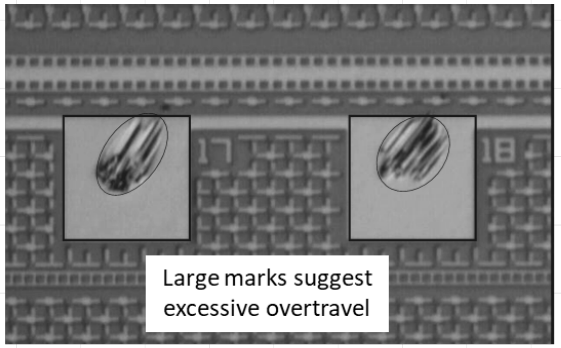
Source: Accretech; SWTest Archives

Example: Probe to Pad Mis-Alignment Due to Debris

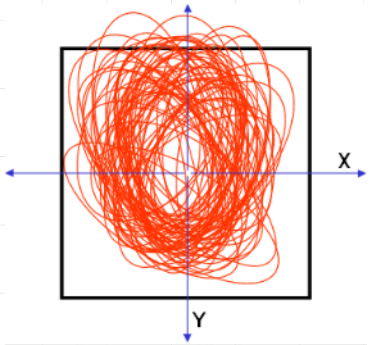
- Precise positioning is critical for small pads of scribeline and test structures.
- Example: Probe-to-Pad Alignment for 32um x 32um pads.
- Poor PTPA will affect the XY location on the pad.
- Poor PTPA will affect the scrub length at overtravel



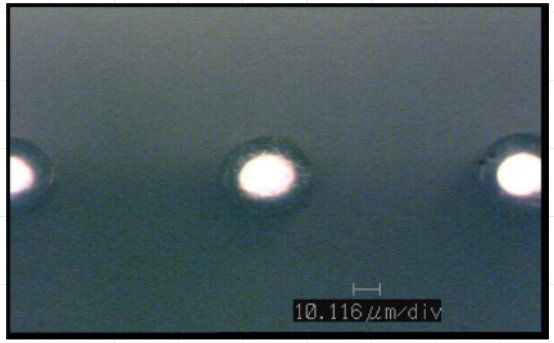
Accumulated Probe Tip Debris Affects PTPA



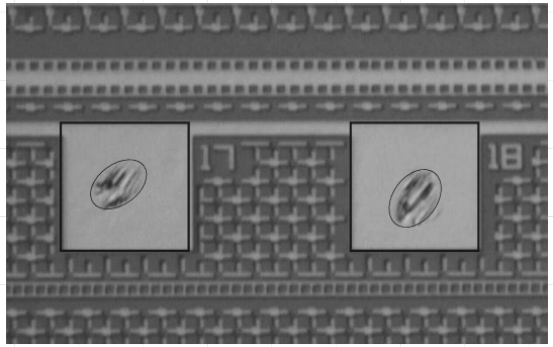
Mis-alignment Due to Poor PTPA



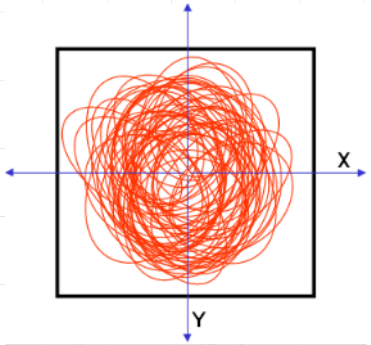
"Super Pad" Shows Poor Alignment



Probe Tip Debris Removed Improved Recognition



Alignment For Small Pad Probing



"Super Pad" Shows Centered Alignment

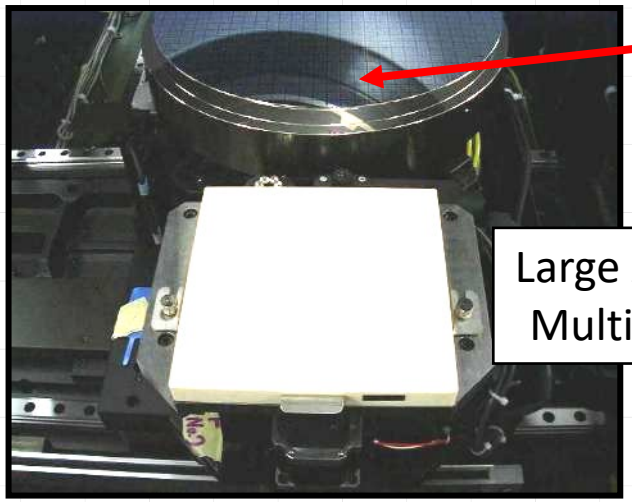
Source: J. Broz, IEEE ICMTS Conf. 2012

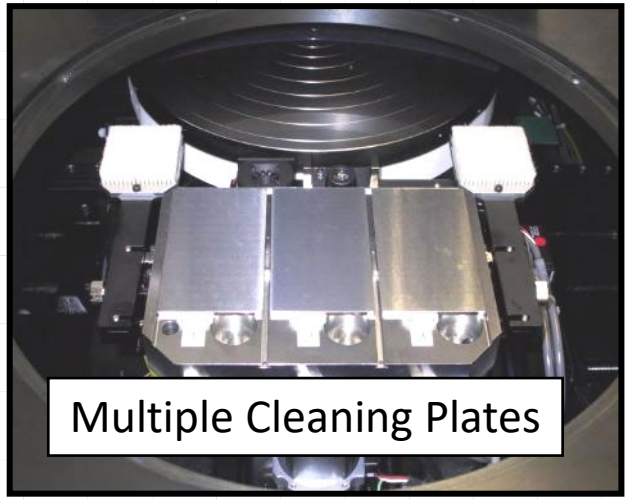
2nd Function of Prober = Probe Cleaning

- Probers have a dedicated cleaning area where the probe card is brought into contact cleaning wafer or cleaning pad to remove tip contamination.

- Cleaning cycles are programmed based on the number of "touchdowns" to optimize cleaning efficiency.

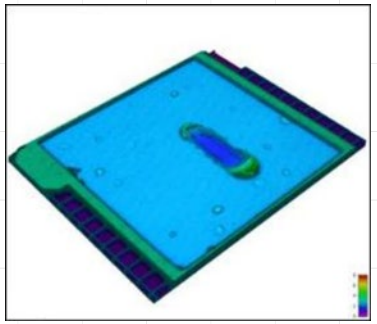
- Advances in cleaning execution performance
  - Profiling for surface recognition and consistent cleaning overtravel
  - Multi-zonal cleaning for recipe optimization
  - Efficient stepping patterns and translation during execution

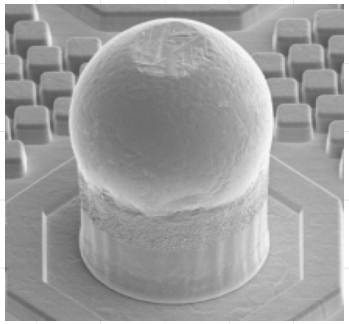




Source: Accretech

Contamination | Film Resistance and Debris

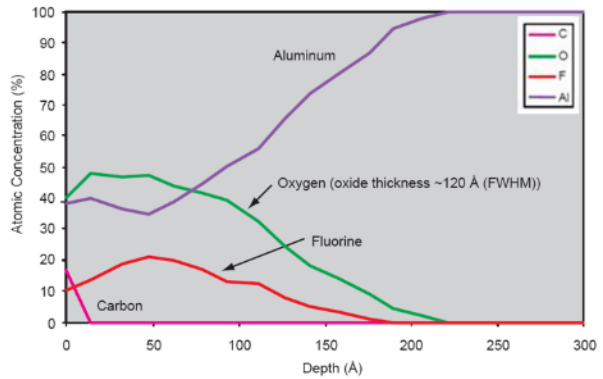




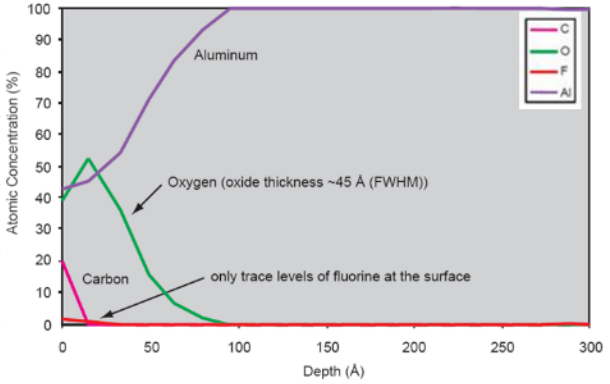
- Pad and Bump metallization affects debris generation
- Pad material and oxides adhere to probe tip.
  - Thick soft metal sticks to probe tips
  - Thin, brittle metal generates debris.
- Build-up of non-conductive layers creates contact reliability issues.

Source: J. Broz, SWTest 2014

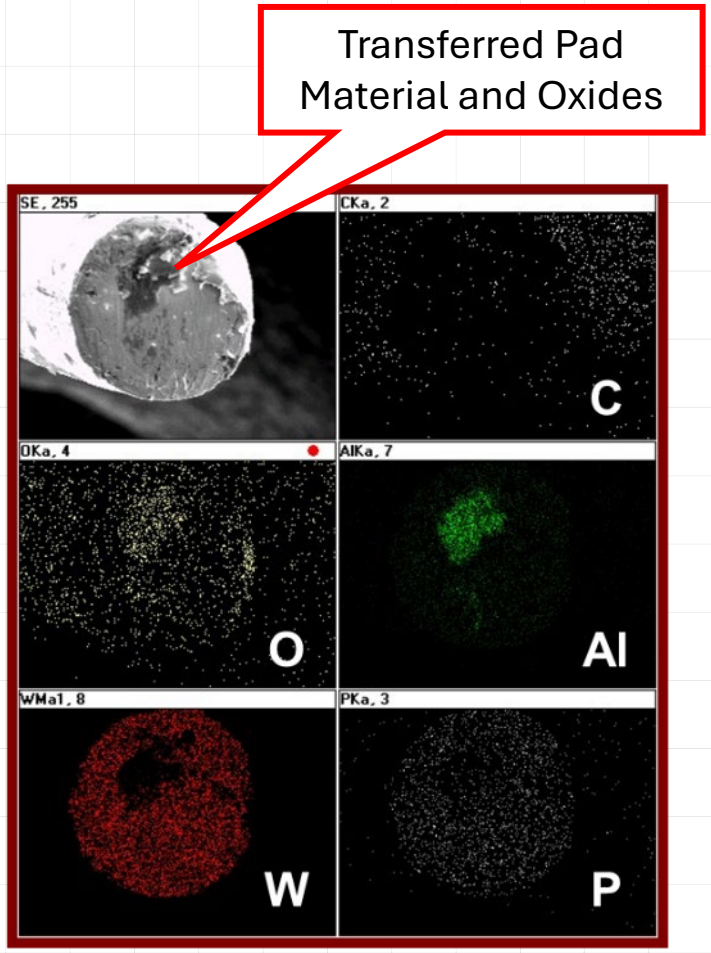
Not so "Clean" I/O Pad : Very difficult to probe



"Clean" I/O Pad : Stable electrical contact



Source: EAG Bond Pad Analysis



Source: J. Broz, SWTest 2007; J. Broz, IEEE ICMTS 2012

Probe Challenges | Reliable Contact

- **Probes touch the DUT, but Current Might NOT Flow !**
- **Probe cleaning is critical for controlling contact.**

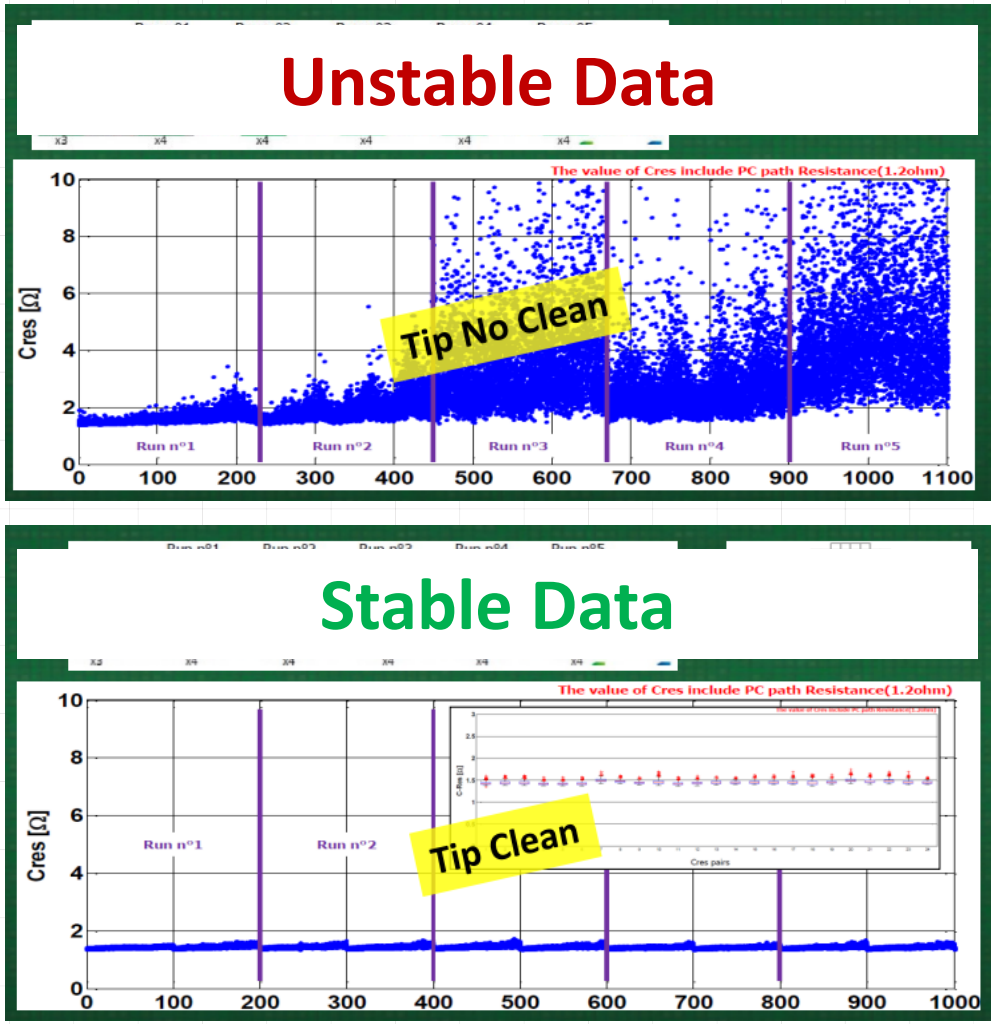
METALLIC CONTACT

$$C_{RES} = \frac{(\rho_{probe} + \rho_{pad})}{4}\sqrt{\frac{\pi H}{P}} + \frac{\sigma_{film} H}{P}$$

Film Resistance

- ρ_{pad}, ρ_{probe}, σ_{film} = resistivity values
- H = hardness of the pads, bumps, pillars, etc.
- P = contact pressure applied by probe

Implement efficient cleaning
to ensure reliable electrical contact.



Source: R. Vallauri, D. Perego, M. Prea, J. Kim, and J. Yun, SWTest 2017

Overview & Agenda

Gel-Pak | Delphon Snapshot

Probing is a “Contact” Sport

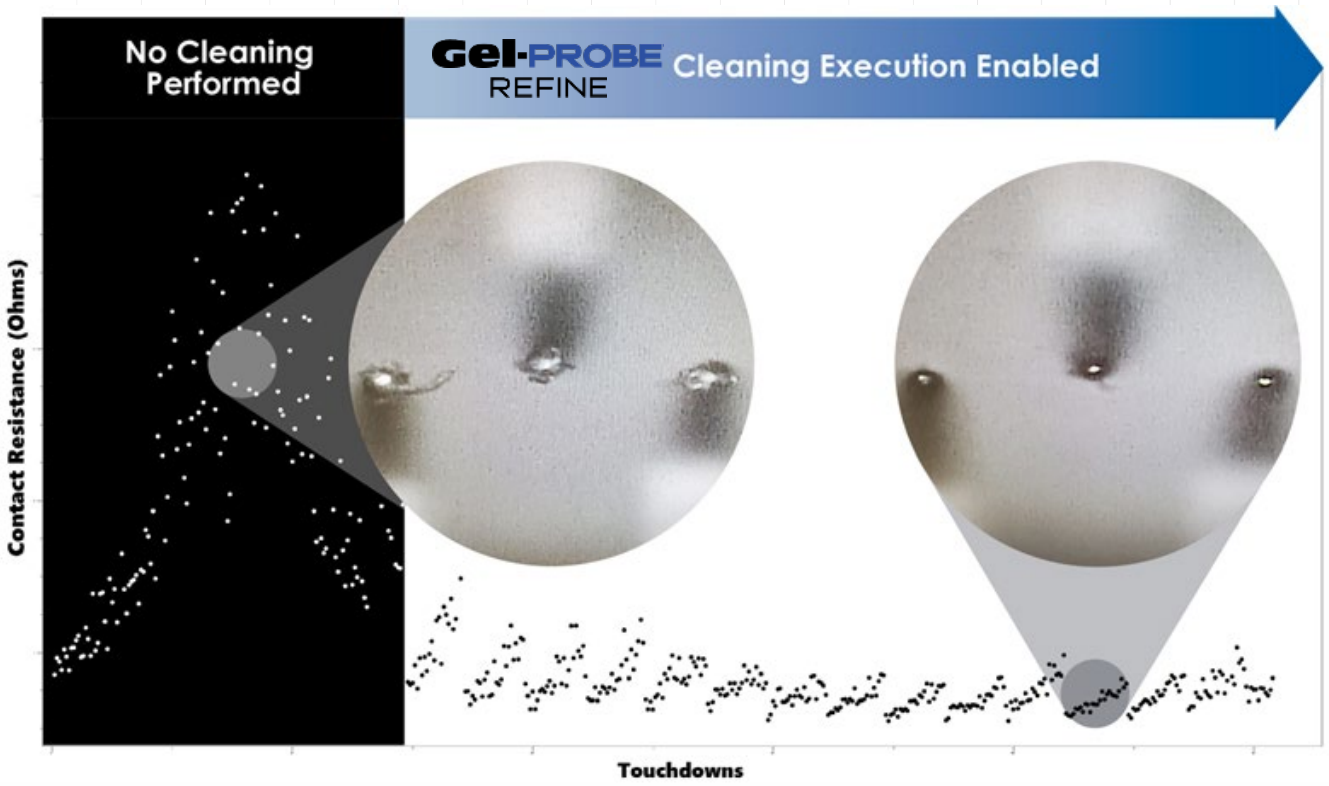
Probe Cleaning is Mandatory | Maximize OEE

Gel-Probe for Efficient Probe Cleaning

Customer Case Studies | Qualifications

Summary & Takeaways

Cleaning is Mandatory



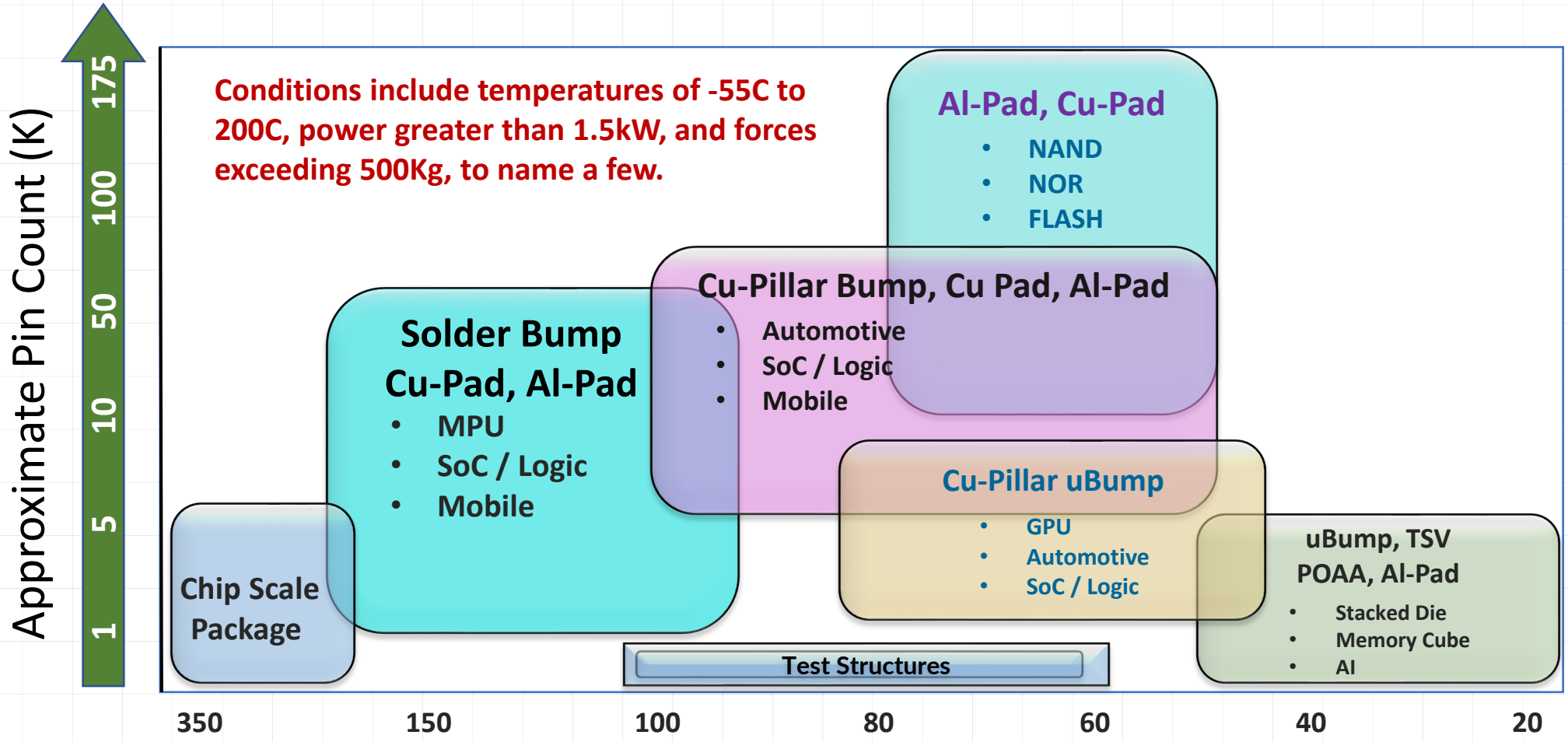
OEE Loss Occurs during Continuous Probing without a Cleaning Process

Efficient Probe Cleaning:

- **Improves test accuracy**: Removes debris, oxides, residuals, etc., that affect test program performance.
- **Increases prober availability:** Assures accurate probe-to-pad-alignment (PTPA) critical for small tips, small device I/Os, fine pitches, and large contactors.
- **Prolongs probe card life**: Consistent cleaning maintains performance and reduces offline repair.
- **Reduces risk of contamination**: Prevents probe-related debris from dropping onto the wafer and affecting subsequent processing steps.

Source: V. Tran, et. al SWTest Asia 2023; J. Broz, FFI COMPASS 2024

All Probes and Probe Card Must be Cleaned



Source: SWTest Archives

Probe Cleaning

- Cleaning Unit or Wide Area Polish Plate (WAPP)
  - Cleaning execution frequently and quickly with small reductions in throughput
  - Size limitation when cleaning large area array probe cards
- Cleaning Wafer
  - Compatible with large area probe cards
  - Long cleaning cycle times due to loading, profiling, unloading, and reloading operations

	Cleaning Unit	Cleaning Wafer
Size	△	◎
Throughput	◎	△
Cleaning Timing	◎ (Any time)	△ (Between wafers)
Upgrade	△ (Hardware & software)	◎ (Software only)

Source: Accretech

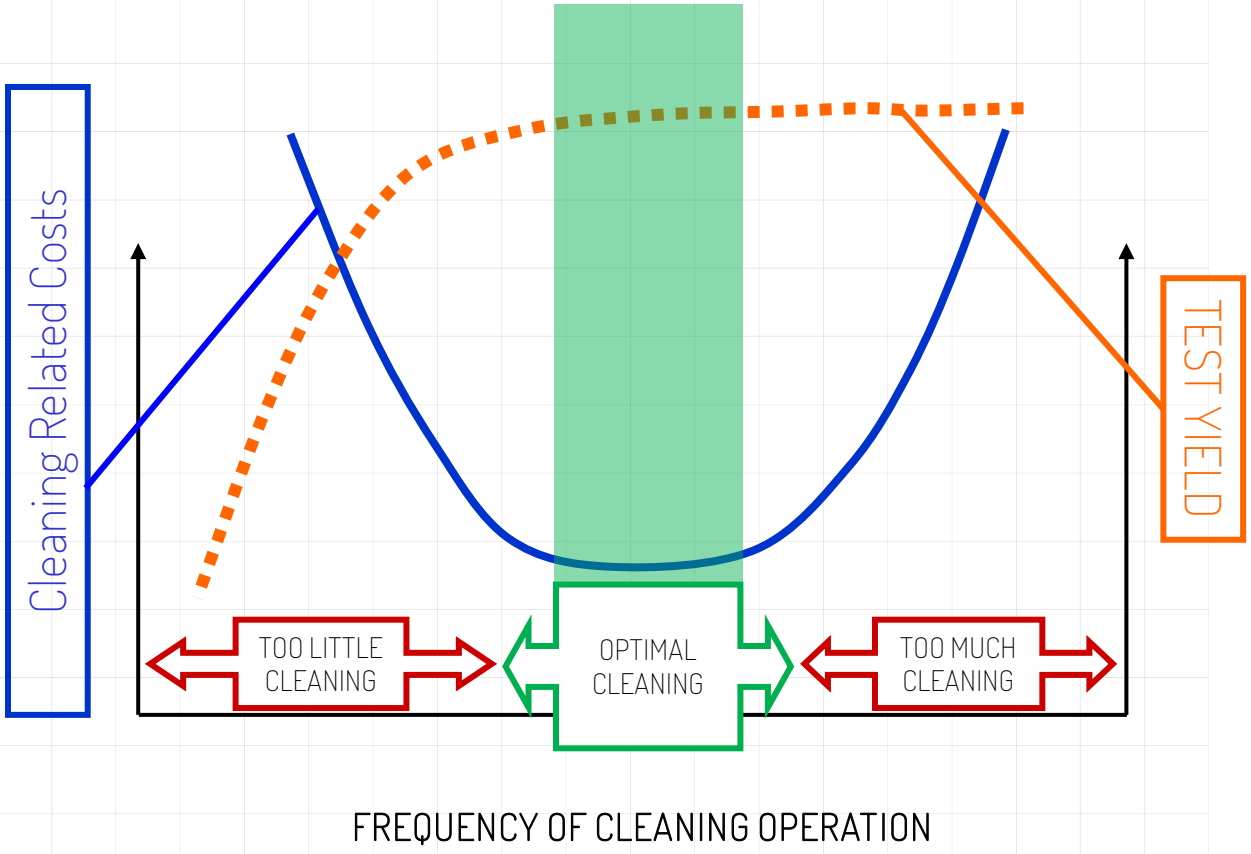
When to Clean ?

- **Usual Answer = <u>IT DEPENDS on the process!</u>**
  - Cleaning can consume > 95% of a probe card lifetime
  - During non-optimized cleaning, test costs increase.

- **Reality = <u>Clean on some type of fixed Schedule!</u>**
  - Focus on CRES sensitive devices (with minor optimization).
  - Problem = Process yields are acceptable, but the process is not optimized (extra costs).
  - Solution = Optimized cleaning materials and procedures that best suited for probe applications.

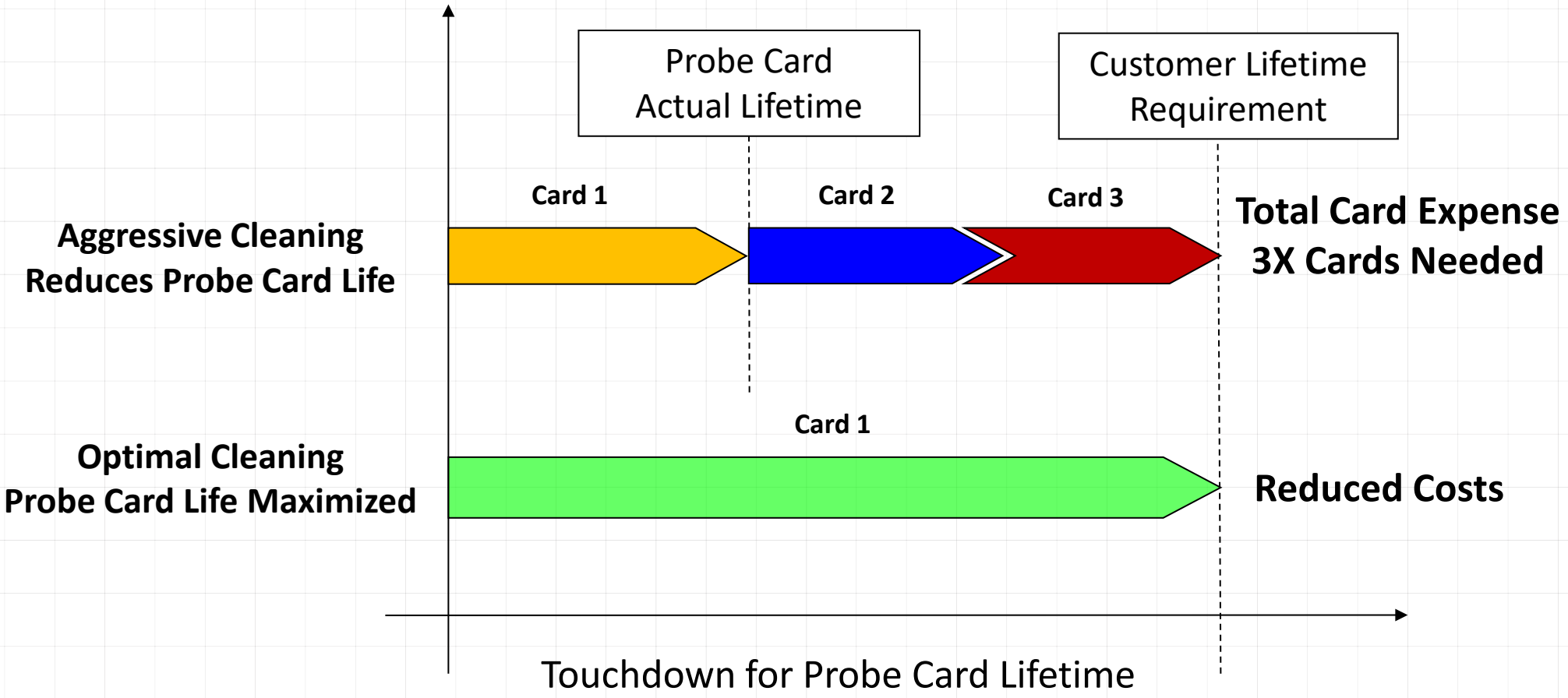
- **Better Answer = <u>Clean only when necessary!</u>**
  - Real time data monitoring of electrical and binouts to assess and define a device specific recipe
  - Problem = Each product requires a dynamic clean recipe.
  - Solution = Adaptive Probe Cleaning (APC) using A.I. Technology

  … *(H. Sugimura, et. al, Advantest VOICE – 2022)*



Source: J Broz, SWTest 2007; J. Broz and V. Tran, SMTA – WLPS 2024

Cleaning Challenge | CRES & Probe Lifetime



Source: J Broz, SWTest 2007; J. Broz and V. Tran, SMTA – WLPS 2024

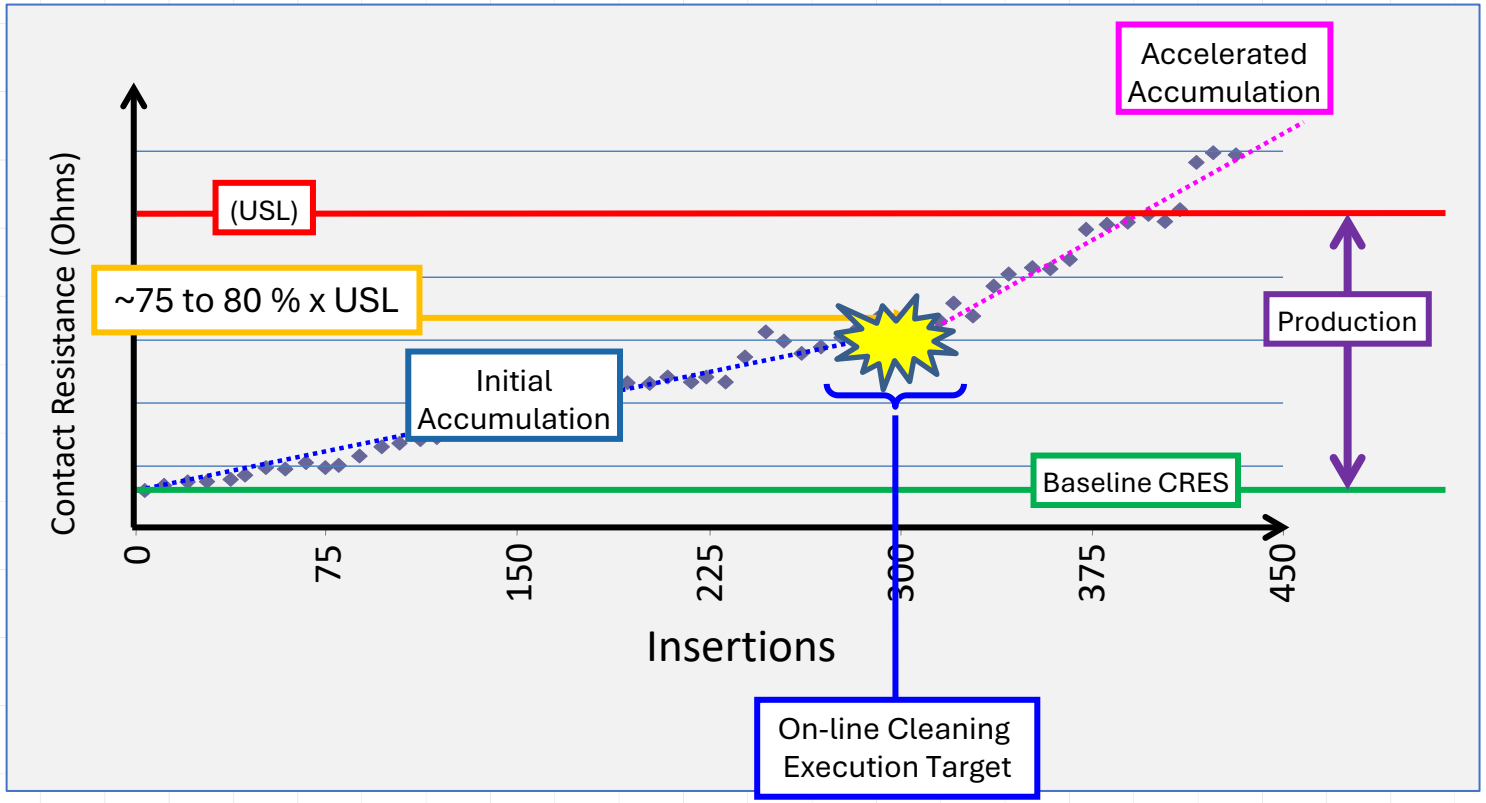
Baseline Recipe Development

- Determine cleaning interval to maximize contact and electrical stability

“Rule of Thumb”

Execute a cleaning at ~75 or 80% of CRES Specification Limit

Example of a Cleaning Strategy Development

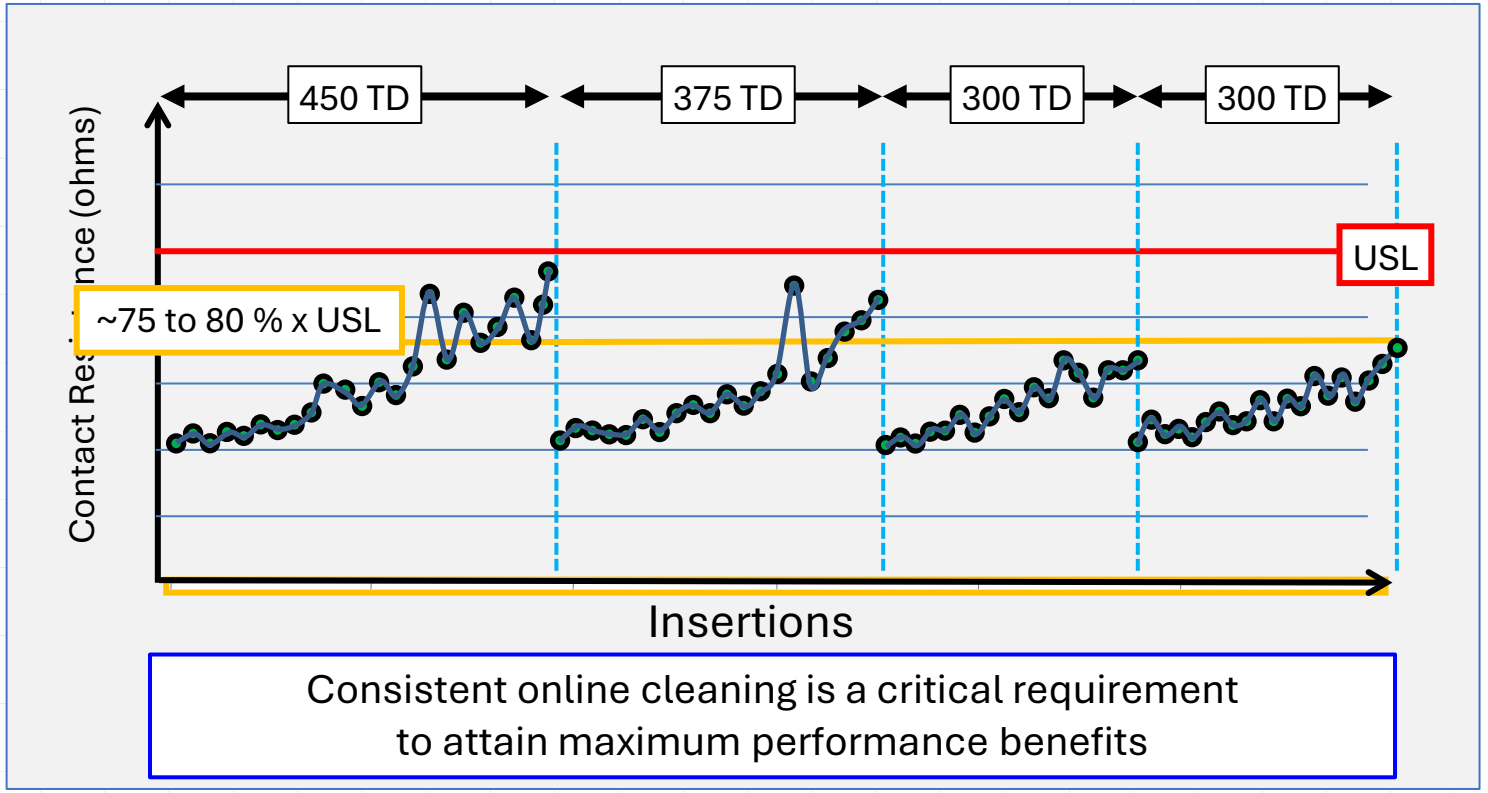


Source: J. Broz, IEEE SWTest 2007; J. Broz BiTS Workshop 2013

Optimizing the Frequency

- Determine the number of TDs per cleaning cycle
  - Depends on the dirtiness (debris, contaminations, etc.).
  - Cleaning OD is based on the probecard supplier recommendations and is typically similar to the probing / programmed overtravel (POT).
- Determine the optimum cleaning material lifespan
  - Indexing between clean TDs is important to prevent over-utilization
  - Over-saturation will affect cleaning efficiency.
  - CRES will be affected by over-saturated working surface,

Example of Defining a Cleaning Strategy Development



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Collaborative Development | GP Probe Cleaning

Gel-Pak had collaborated with FormFactor (and others) on the original GEL cleaning wafers/sheets and core IP development in 1990s.

In 2023, Gel-Pak collaborated with key customers to define critical material and performance properties to restart the product line.

Backed by 40-years of materials processing and formulation experience Gel-Pak scientists rapidly developed and improved advanced prototypes based on prior work.

Gel PROBE REMOVE

Gel PROBE REFINE

With global manufacturing footprint, Gel-Pak is positioned as a collaborative, high-volume supplier of cost-effective probe cleaning products.

Efficient Cleaning | Elastomer Cleaning Materials

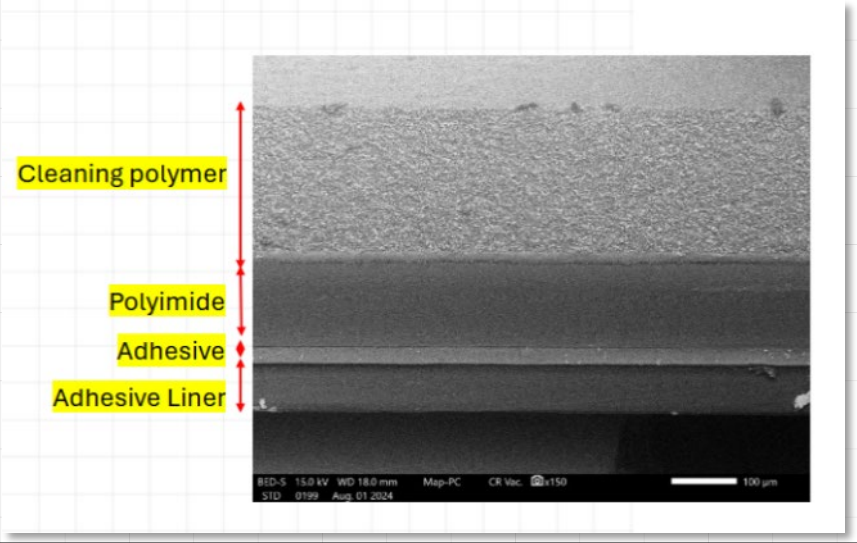
Property	GP Probe ReFine GP Probe ReMove
Chemistry	Gel Elastomer
Color	Green-Gray (filled) Opaque (unfilled)
Surface Texture	Proprietary "Dull Surface" for Optical Recognition
Abrasive Particle Filler	3um Silicon-Carbide (SiC) w/ Particle Size Distribution
Sheet Substrate	Polyimide (High and Low Temperature Capable)
Outgassing	Meets and Exceeds ASTM E595 TML ≤≤ 1.00% and CVCM ≤≤ 0.10%
TTV	Less than 25um
Sheet Film Tolerance	±20um
Operating Temperature	-60C to 200C

Standard Cleaning Wafers

SEMI 200mm and 300mm

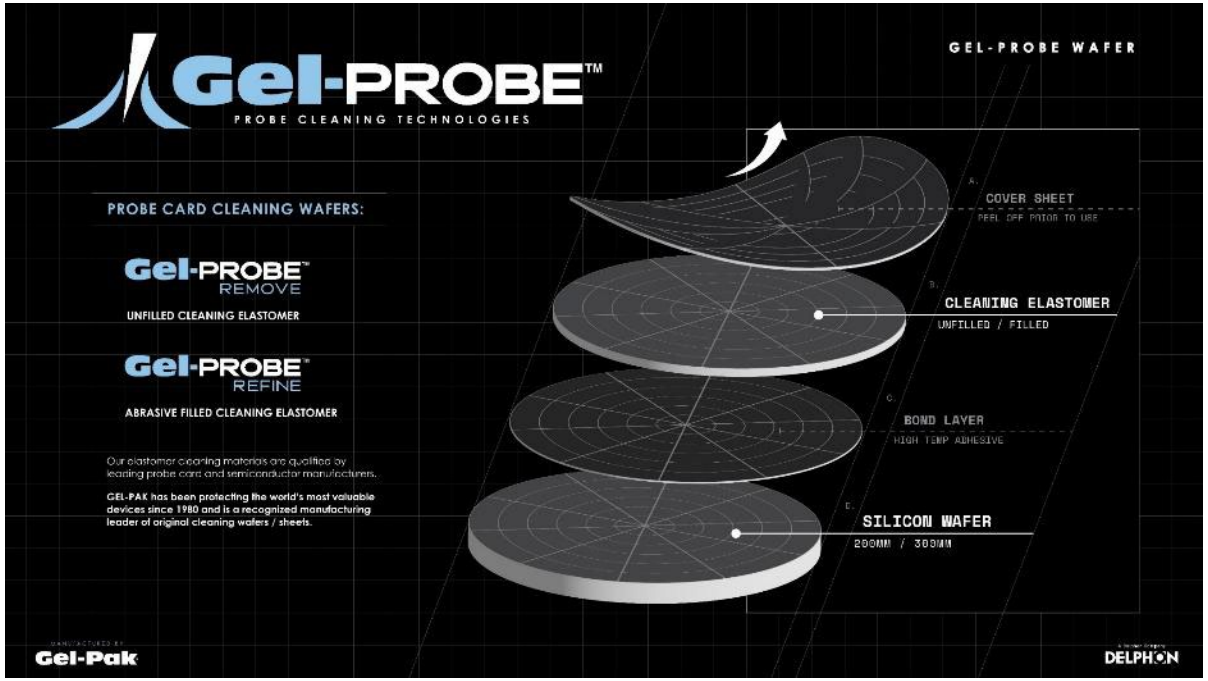
Polyimide backed sheets

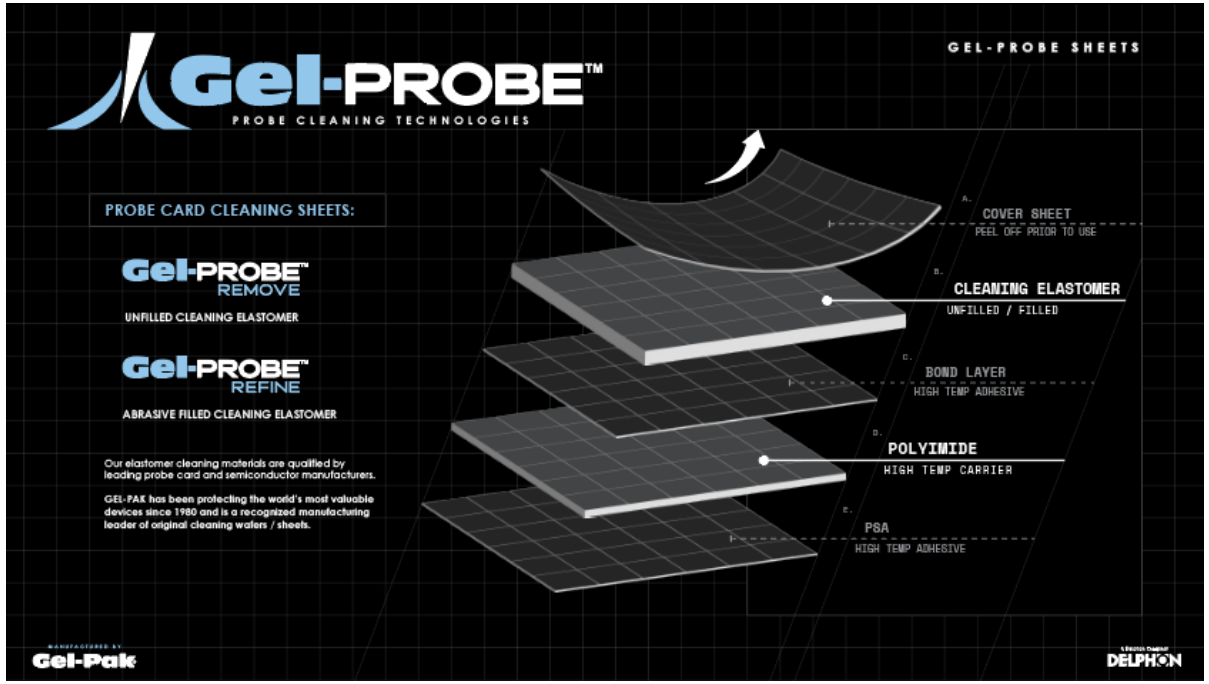
-60˚C to 200˚C performance



Engineered with a variety of abrasive loadings

Operating Temperature Range = -60C to 200C





Increased loading → Increased material hardness → Increased Cleaning Efficiency

Gel-PROBE REFINE

Available in a variety of abrasive loadings

Increased loading → Increased material hardness → Increased Cleaning Efficiency

		Loading				
		none	70	99	150	300
	Loading					
ReMove (GPM)	none	0	x	x	x	x
ReFine (GPF)	3um, SiC	x	L3	M3	H3	U3
	5um	x	L5	M5	H5	x
	10um	x	L10	M10	H10	x
	15um	x	x	x	x	x
ReCover (GPC)	3um	x	x	x	x	x
	5um	x	x	x	x	U5
	10um	x	x	x	x	U10
	15um	x	L15	M15	H15	U15

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- **Case 1 = HVM Implementation**
  - ReFine H3 Qualification on a 300mm Cleaning Wafer
  - HVM “Drop-In” Validation
  - First Pass Yield Improvement

- **Case 2 = Celadon Production Parametric Probe Card**
  - Replace incumbent material with viable 2nd source
  - Confirm electrical stability and performance recovery
  - Maintain tip shape and scrubbing performance
  - Exceed lifetime target of cleaning 10M TDs

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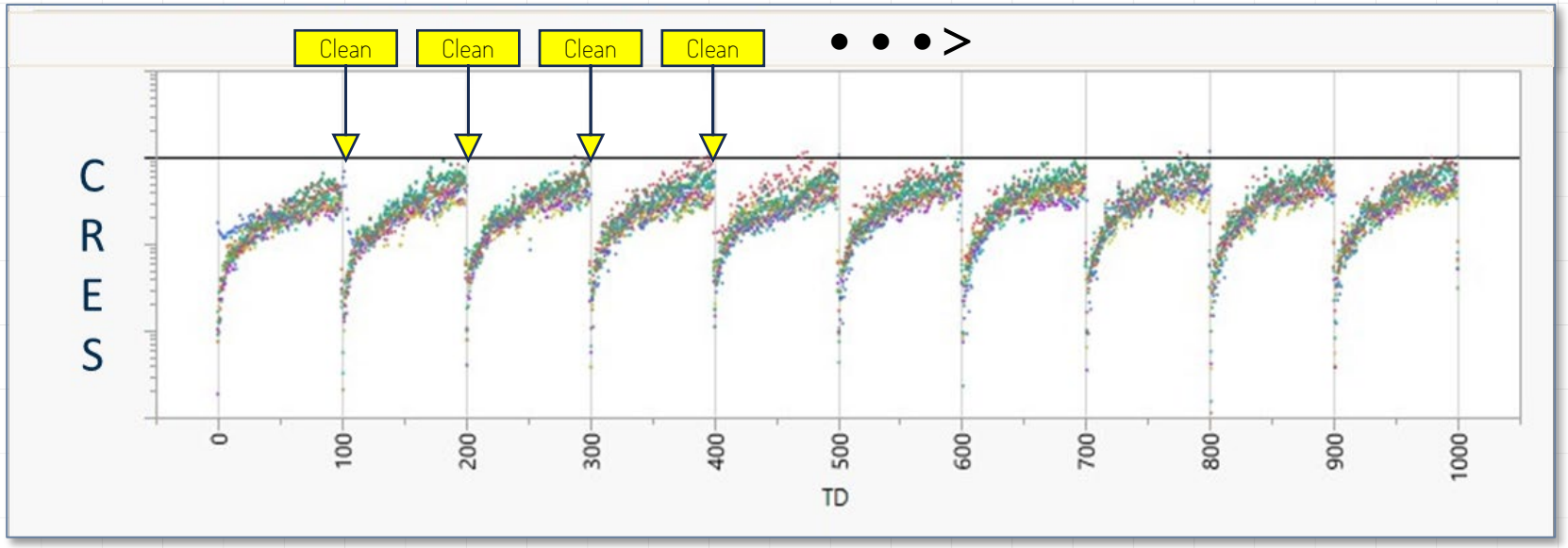
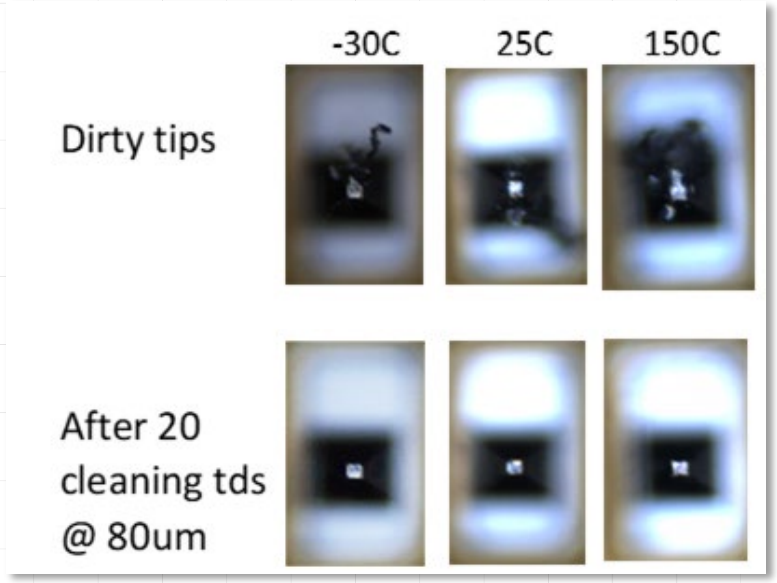
GP-ReFine H3 Qualification

- Successful qualification at Top 4 Memory Probe Card Suppliers
  - Rapid, Stable CRES Recovery (~20%)
  - Reduced Tip Wear (~15 to 25%)
  - Improved Cleaning Efficiency (~30%) at T ≤ -30C and T ≥ 125C
  - Minimal debris generation during long-term assessment.

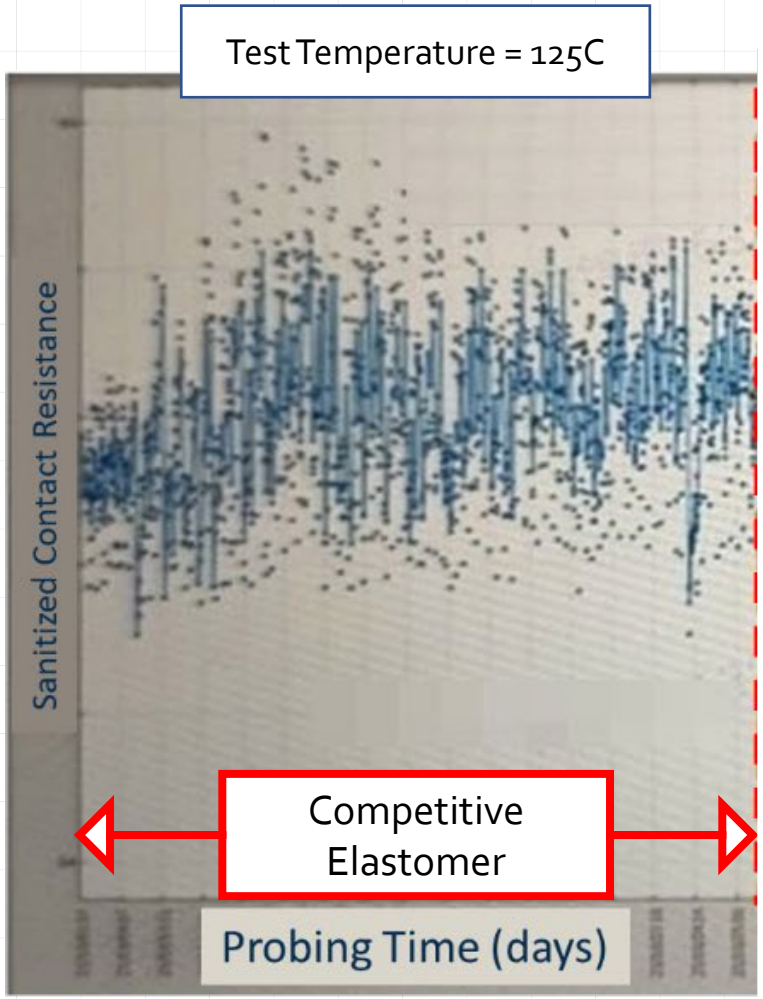




HVM "Drop-In" Validation

A consistent 1% yield improvement can translate to
- *$150M/year net profit gain to a logic fab*
- *$110M/year net profit gain at a NAND fab.*

Source: W. Yang, SEMI Silicon Valley Forum, 2019



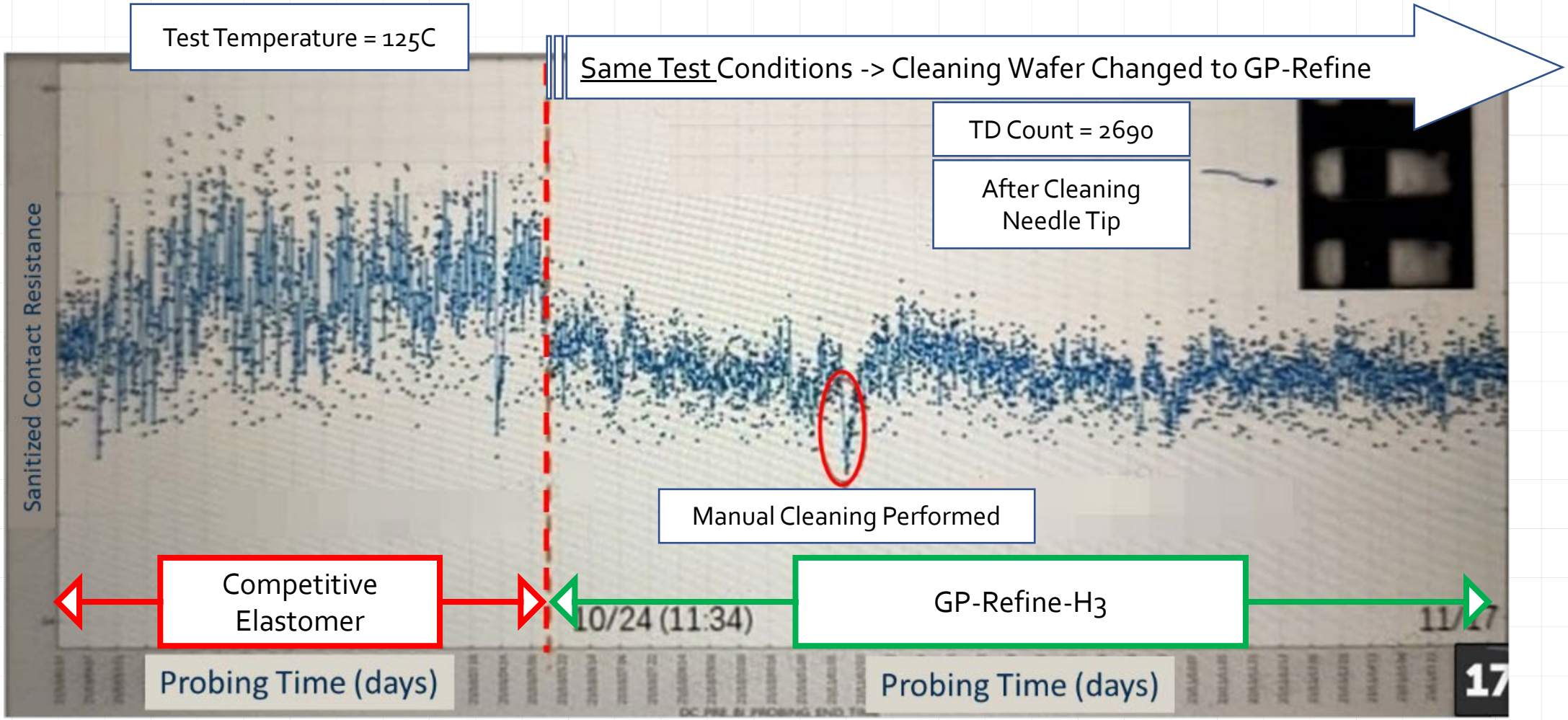
- Customer was using a competitive product with a large area, memory probe card.
- GP ReFine Cleaning Wafer installed into test cell
  - Cleaning recipe unchanged
  - Test program was unedited
  - Prober was not adjusted
  - CRES / test program monitored
- Immediate performance improvement attained and sustained for 4-weeks during qualification.

Source: J. Broz, FFI COMPASS 2023

HVM "Drop-In" Validation

A consistent 1% yield improvement can translate to
- *$150M/year net profit gain to a logic fab*
- *$110M/year net profit gain at a NAND fab.*

Source: W. Yang, SEMI Silicon Valley Forum, 2019



Source: J. Broz, FFI COMPASS 2023

Customer Case Studies

- **Case 1 = HVM Implementation**
  - ReFine H3 Qualification on a 300mm Cleaning Wafer
  - HVM “Drop-In” Validation
  - First Pass Yield Improvement

- **Case 2 = Celadon Production Parametric Probe Card**
  - Replace incumbent material with viable 2nd source
  - Confirm electrical stability and performance recovery
  - Maintain tip shape and scrubbing performance
  - Exceed lifetime target of cleaning 10M TDs

Qualification Overview

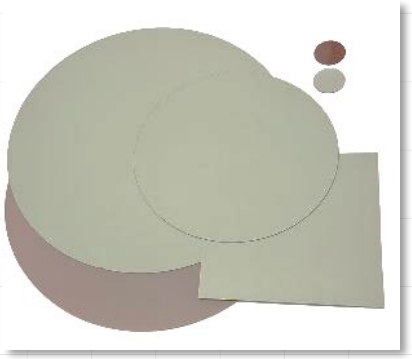
- **Materials**
  - Probe Card: VC20 ELEMENT SERIES
  - Prober Type: CPS APEX 200mm prober
  - Primary Cleaning Material: Gel-Probe ReFine-H3
  - Abrasive Cleaning Material: CWC (Celadon Tungsten Carbide)

- **Probe Card Parameters**
  - Virtual Pad Size Target: 40um x 40um
  - Probe Array: 1 x 16 (dual approach)
  - Probe Pitch: 126um pitch
  - Average Probe Tip Ø: 10µm
  - Test Overdrive (OD): 30 to 40um

- **Test Parameters (**w/recommended cleaning recipe**)**
  - Blanket Aluminum Wafer (DUT)
    - Touchdowns @ 40µm OD (electrical contact ±4um)
  - GP ReFine-H3 (150 loaded)
    - 15 TDs @ 60um OD every 250 DUT TDs
  - CWC (Celadon Tungsten Carbide)
    - 3 TDs @ 40um OD every 50,000 DUT TDs

VC20 ELEMENT SERIES

CPS APEX
200mm Prober



Gel-Probe ReFine-H3

Celadon Tungsten-
Carbide (CWC)

Qualification Plan for Celadon Probe Cards

1. Mimic a customer process using a blanket aluminum wafer
   - Verify elevated and unstable CRES can be achieved.
   - Visualize and assess scrub marks

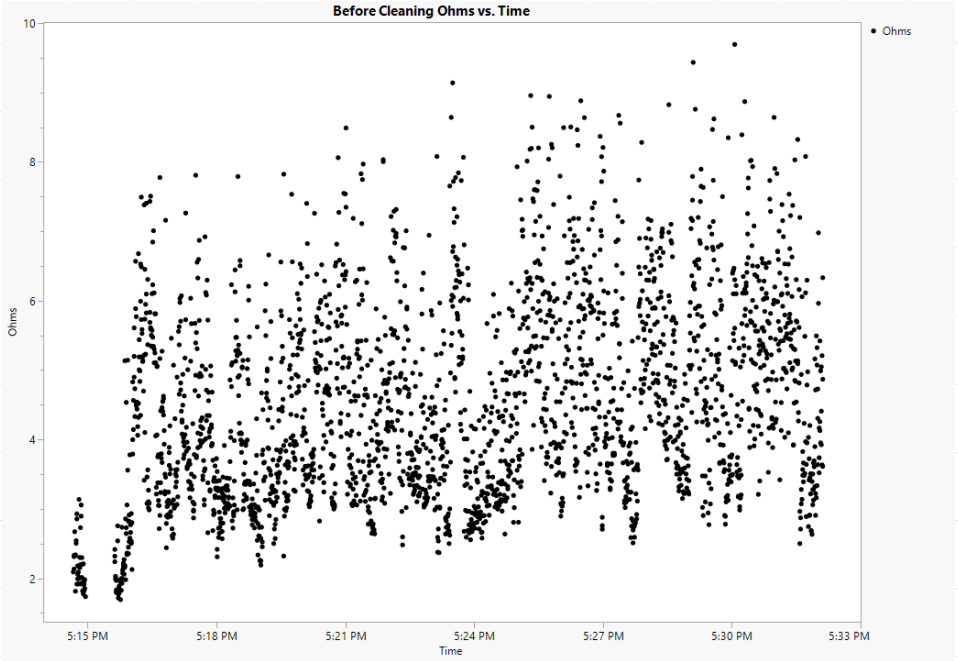
2. Confirm CRES recovery testing with Celadon recipe
   - Probe card is “made dirty” with multiple TDs
   - Cleaning performance is demonstrated.

3. Wear testing with cleaning execution
   - “Long term” tip wear
   - Tip shape change
   - Exceed 10M Al-TD (with cleaning) target
   - Scrub length assessment (virtual pad)

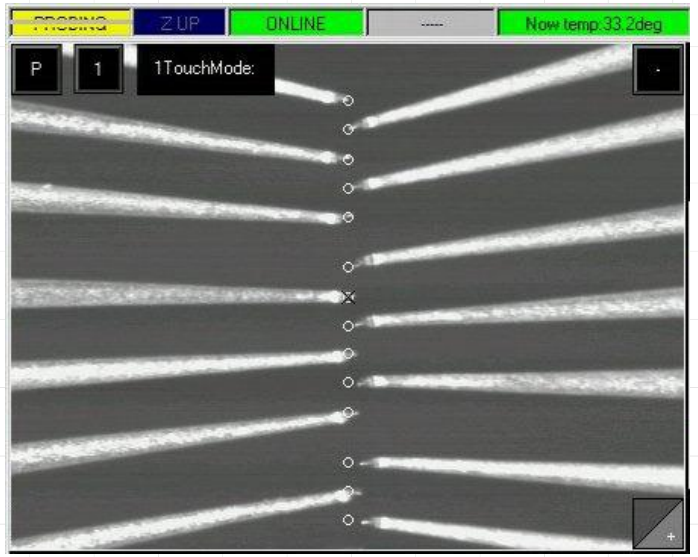
4. Qualification // Verification
   - Authorized cleaning material options
   - Cleaning recipe guidelines

Qualification Plan

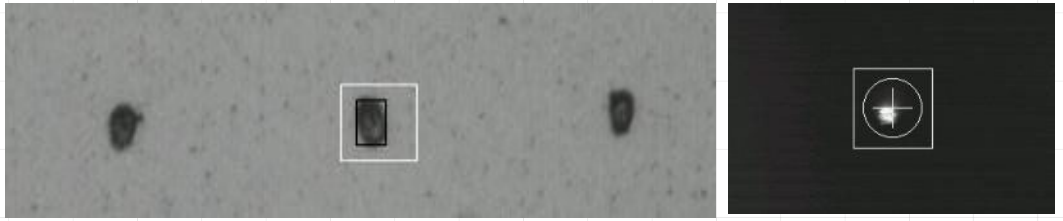
1. Mimic a customer process using a blanket aluminum wafer
   - ✓ Verify elevated and unstable CRES can be achieved.
   - ✓ Visualize probes and assess scrub marks.

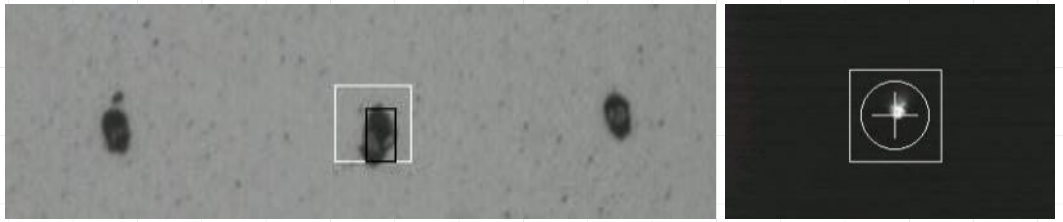


~2500 TD without cleaning show CRES instability



Probe 4

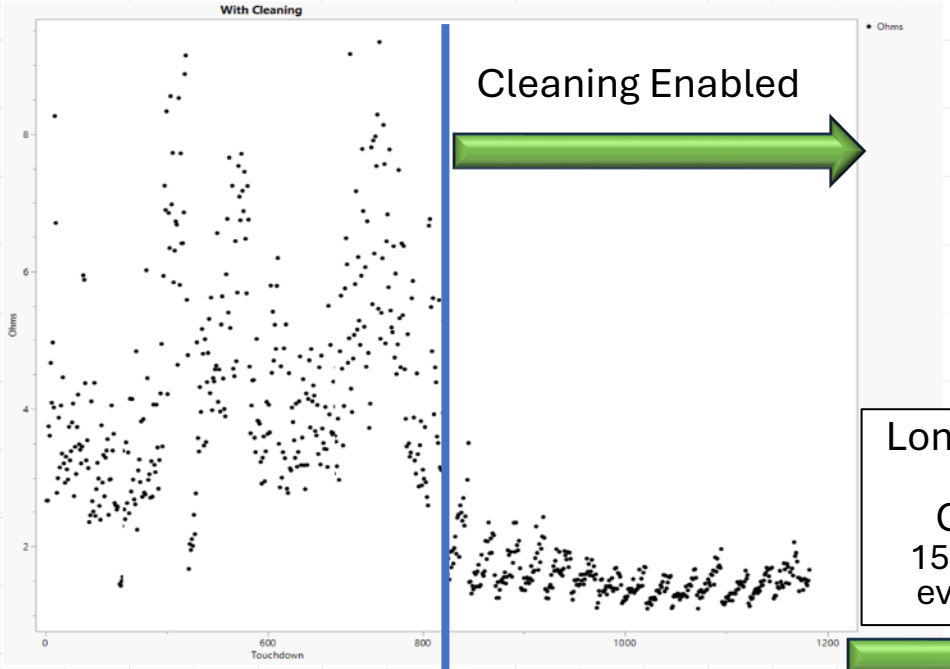




Probe 14

Qualification Plan

2. Confirm CRES recovery testing with Celadon recipe
   - ✓ Probe card is “made dirty” with multiple TDs.
   - ✓ Cleaning performance demonstrated.

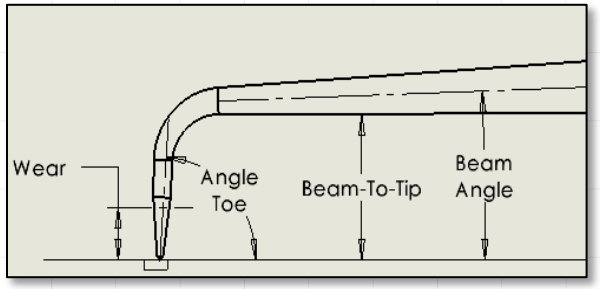


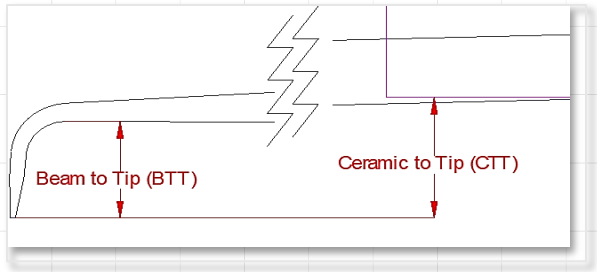
Long Term Cleaning

GP ReFine-M3
15 TDs @ 60um OD
every 250 DUT TDs

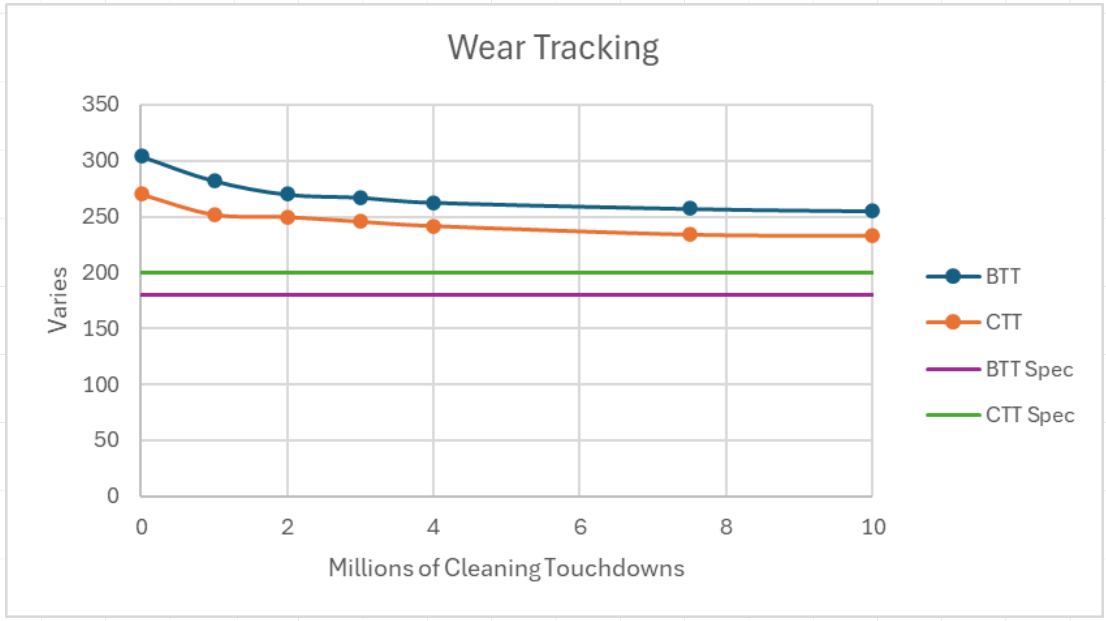
Qualification Plan

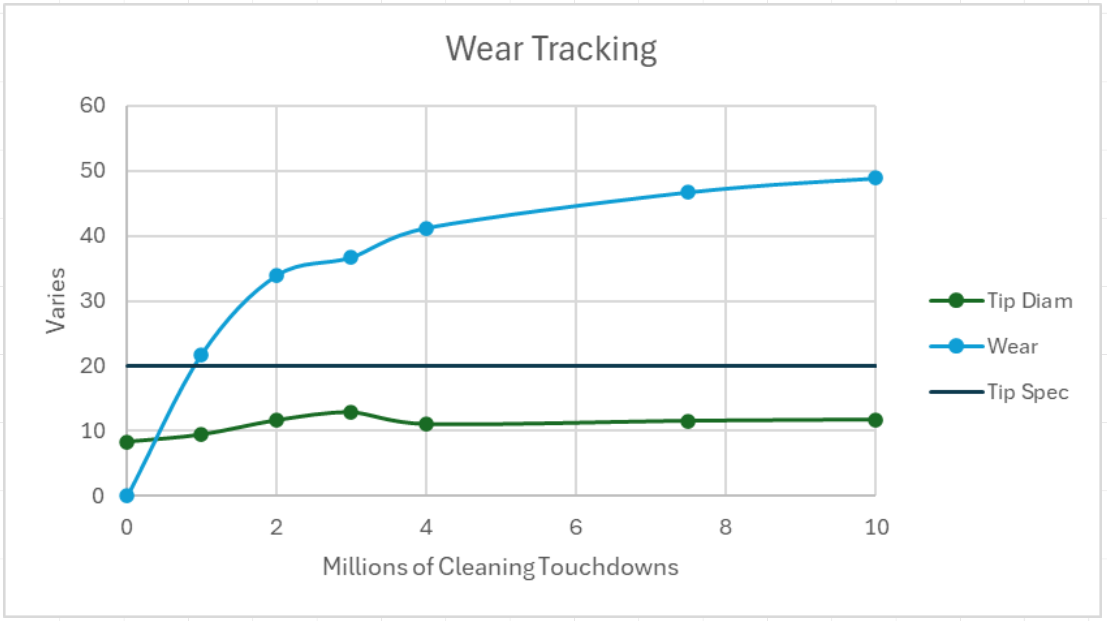
3. Wear testing on cleaning material
   - ✓ "Long term" tip wear
   - ✓ Tip shape change
   - ✓ Exceed 10M Al-TD (with cleaning) target
   - • Scrub length assessment (virtual pad)





- BTT = Beam-To-Tip
- CTT = Ceramic-To-Tip
- Wear = BTT - CTT



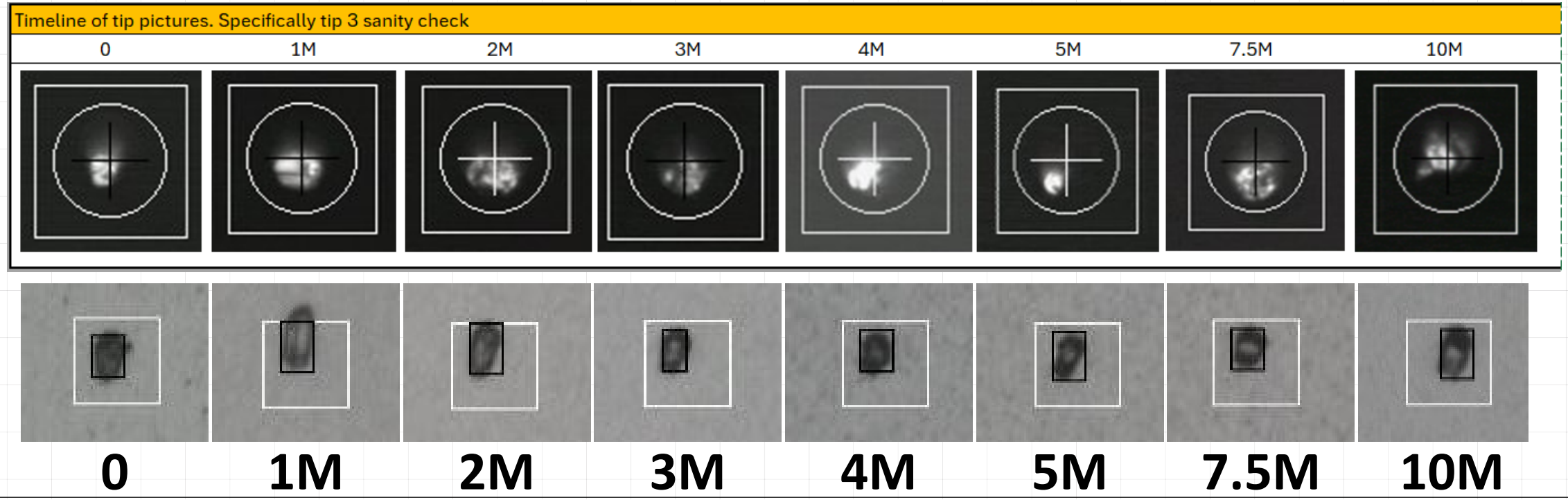


Qualification Plan

3. Wear testing on cleaning material
   - ✓ “Long term” tip wear
   - ✓ Tip shape change
   - ✓ Exceed 10M Al-TD (with cleaning) target
   - ✓ Scrub length assessment (virtual pad)

Gel-Pak GP ReFine H3

- Controls CRES
- Cleans away debris from tip
- Decreases Tip Ø (sharpens)
- Does not decrease BTT
- Probe Lifetime ++10M Cleaning TDs



Qualification Plan

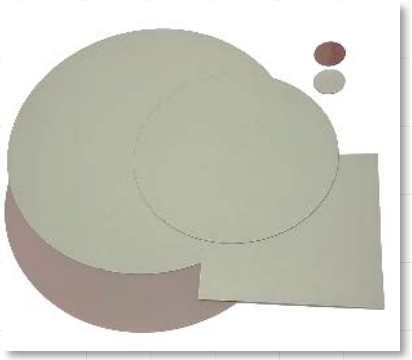
4. Qualification // Verification
   - ✓ Authorized cleaning material options
   - Cleaning recipe guidelines

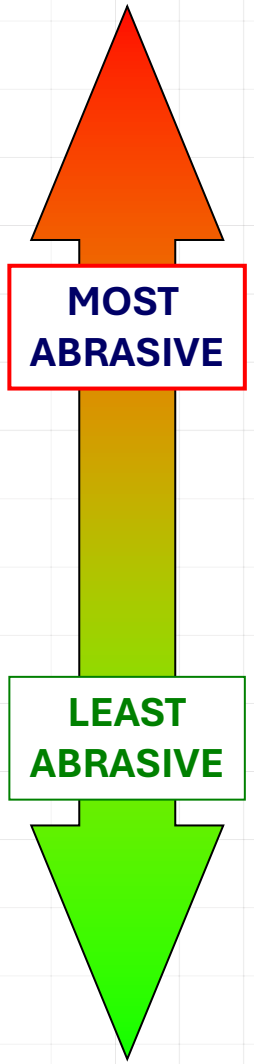
- **CWC (Celadon Tungsten Carbide)**
  - Improve Cres
  - Removes embedded particles
  - Increases Tip Ø (flattens)
  - Decreases BTT
- **Gel-Pak GP ReFine**
  - **Controls Cres**
  - **Cleans away debris from tip**
  - **Decreases Tip Ø (sharpens)**
  - **Does not decrease BTT**
- **Soft Bristled Brush**
  - Cleans away loose debris
  - Might **not** cure Cres issue
  - Will not remove embedded particles)

Gel-Probe ReFine H3

Polyimide backed sheets

-60˚C to 200˚C performance





Qualification Result

4. Qualification // Verification
   - ✓ Authorized cleaning material options
   - ✓ Cleaning recipe guidelines

Gel-PROBE™ REFINE

SUMMARY

- GP ReFine-H3 has been qualified for on-line cleaning and can be implemented to the support cleaning requirements of Celadon Probe Card in various prober systems. For existing customers, GP ReFine-M3 would be a “drop-in replacement” for Probe Polish 99.

- General Guidelines for GP ReFine Elastomer Cleaning Materials:
  - Touchdown up to 30 times in a step array, with at least 75 microns index between steps.
  - Indexing will prevent overuse and excessive damage to the elastomer working surface.
  - Overdrive should be similar and/or the normal test environment.
  - GP ReFine-Sheets will need to be changed on a regular basis.

- Once CRES gets too high and cannot be recovered with elastomer cleaning, it will be necessary to use a CWC™ plate or wafer to remove embedded particles and oxidation.

Overview & Agenda

Gel-Pak | Delphon Snapshot

Probing is a “Contact” Sport

Probe Cleaning is Mandatory | Maximize OEE

Gel-Probe for Efficient Probe Cleaning

Customer Case Studies | Qualifications

Summary & Takeaways

Summary & Takeaways

- **Emerging significant challenges (both technical and commercial) for stable contact are becoming evident as test coverage and complexity increase.**
  - More extensive coverage necessitates earlier wafer probing to assess composite yields.
  - Greater complexity requires probe cards featuring higher performance.

- **Effective cleaning materials and processes are essential to any wafer probe operation.**
  - Cleaning practices directly influence yield, probe card functionality, and overall costs.
  - Poorly optimized cleaning can compromise test results, shorten probe lifespan, reduce throughput, and impact up-time negatively.

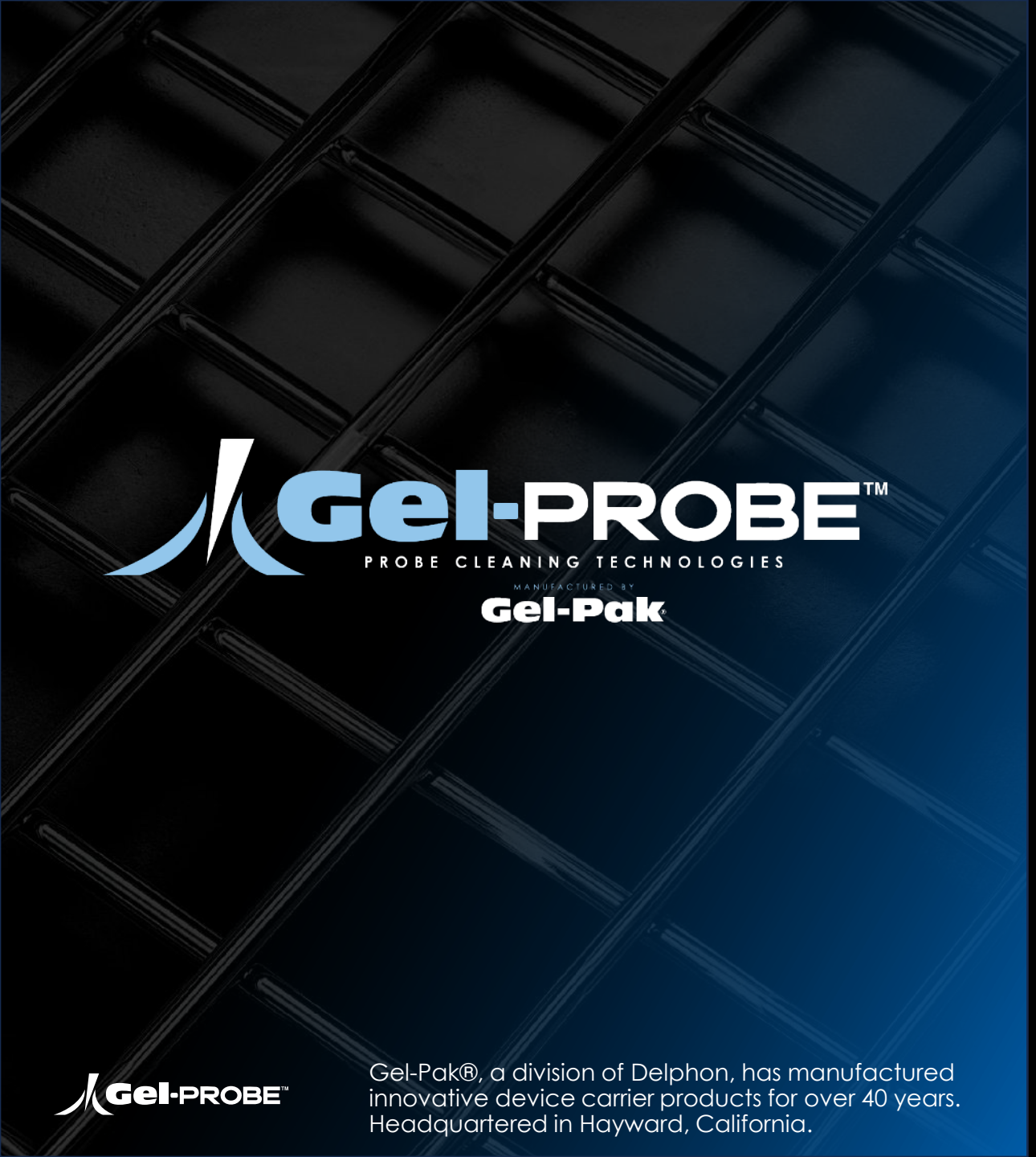
- **Wafer probing across the Lab to Fab ecosystem must not hinder the adoption of new technologies and facilitating cost-effective testing strategies.**

Acknowledgements // Collaborative Partners

- Garrett Tranquillo (Celadon Systems)
- Dalton Roehl (Celadon Systems)
- Michele Jorgensen (Celadon Systems)
- Sancho Adam (Complete Probe Solutions)
- Mike Dean (Complete Probe Solutions)
- Customers and other partners that have asked to remain anonymous.

Questions ?

DELPHON
Merging Innovative Technologies



Gel-Probe Cleaning Technologies

Maximize Yield and Reduce Cost of Test

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Director of Research and Development

Gel-Pak®, a division of Delphon, has manufactured innovative device carrier products for over 40 years. Headquartered in Hayward, California.