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Revolutionary SiC-based Micro-MEMs Cryogenic Probing Solution down to 2K

CUG010

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March 17, 2025

Design and Fabrication of a SiC-based MEMS Probe Die

Gregory N. Nielson, PhD
Nielson Scientific

Motivation and Technical Objectives

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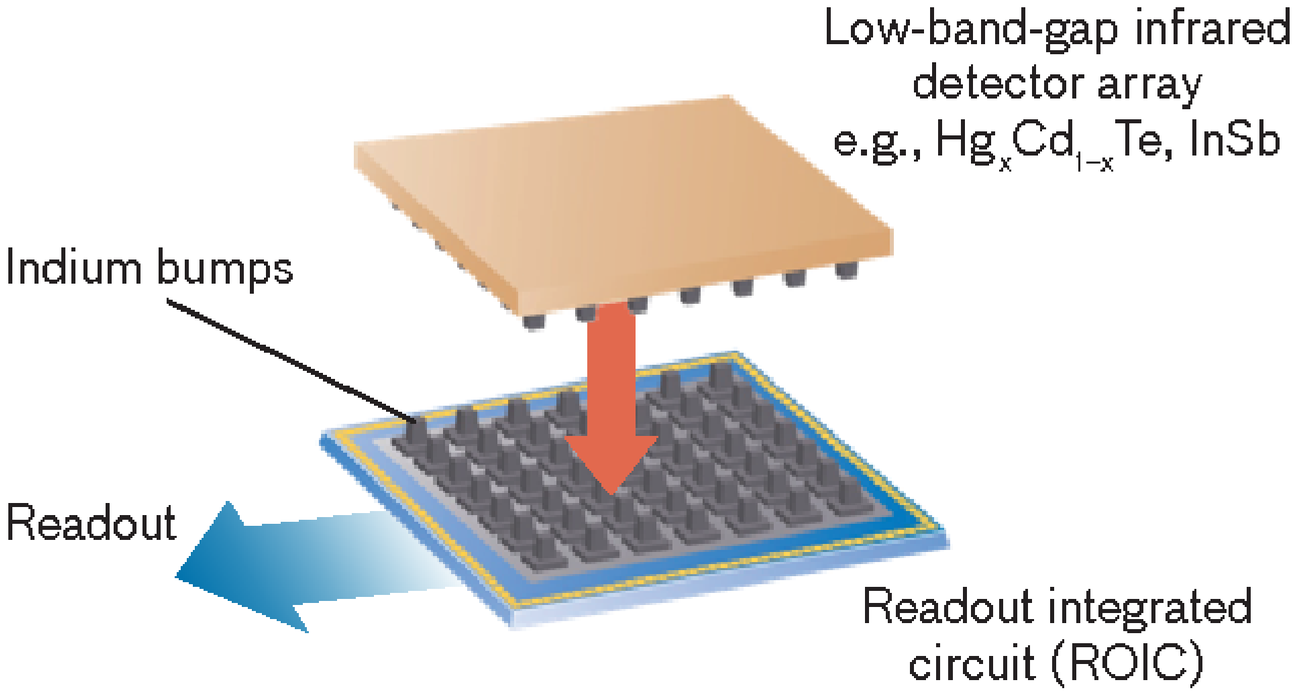
Probe card for testing multiple nearest-neighbor pixels in a cryogenically cooled IR focal-plane array prior to ROIC attachment

- Cryogenic operation
- Probe tip pitch to match pixel pitch
- Transparent probe card for visual alignment
- Tip compliance behavior to match traditional probe tips
  - Tip force of 15 - 40 µN/µm²
  - Tip displacement of 25 - 75 µm at desired tip force



Conceptual Design

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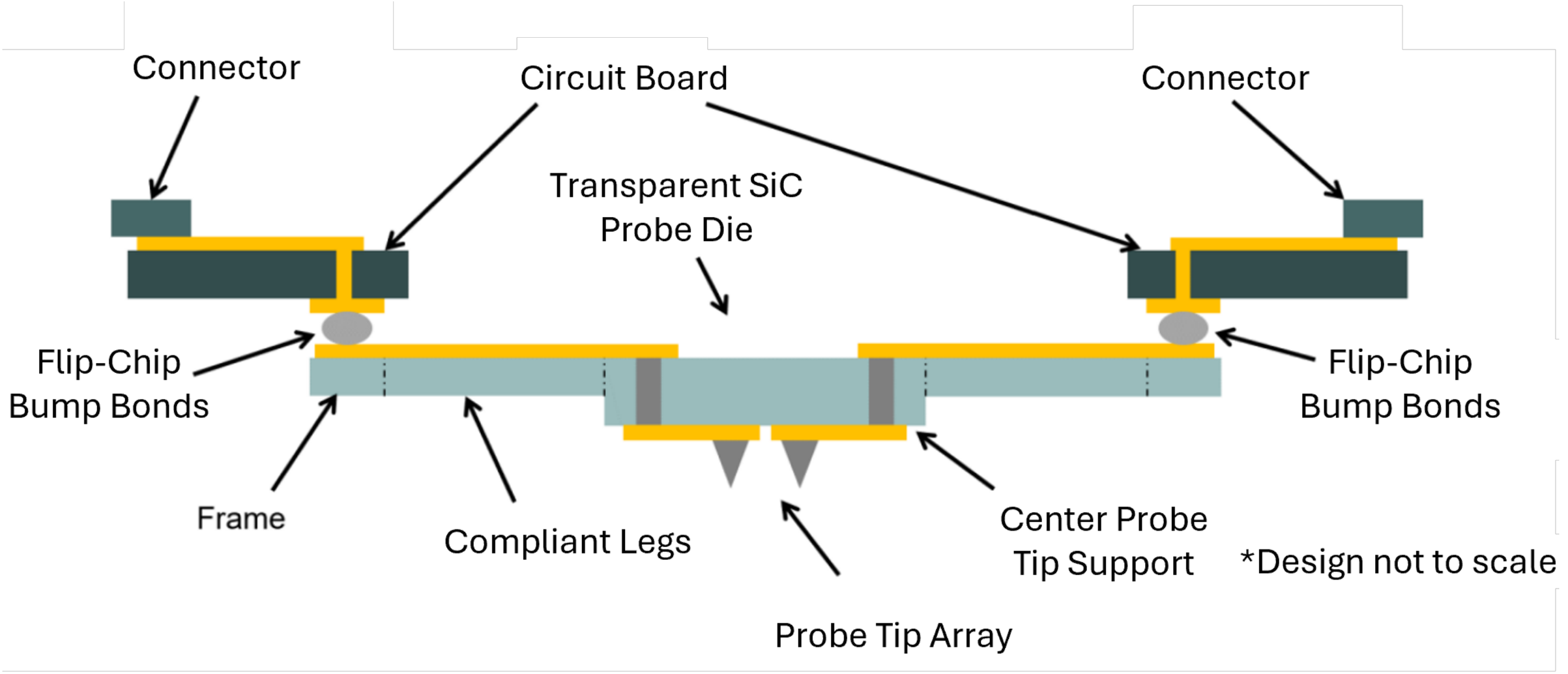
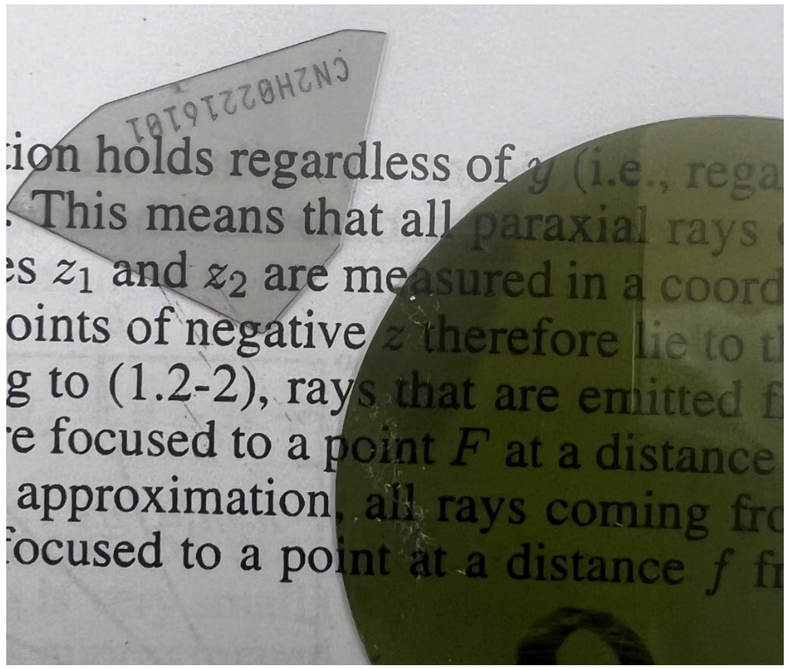


SiC Substrate

Nielson Scientific

Operating Temperature	Tensile Strength	Thermal Conductivity	Density	Young's Modulus	Poisson's Ratio
~1800°C	1.5 GPa	490 W/m*K	3.21 g/cm^3	440 Gpa	0.2

- Very high thermal conductivity
- Chemically inert
- Maintains high strength through operating temperature range
- Wide bandgap semiconductor (3.23 eV)
- Transparent to visible and IR light (~2.7 optical index)
- Extremely hard (9.5 Mohs hardness)
- Low coefficient of thermal expansion
- Robust to radiation
- Very low helium diffusion rates



Probe Card Mechanical Design Concepts

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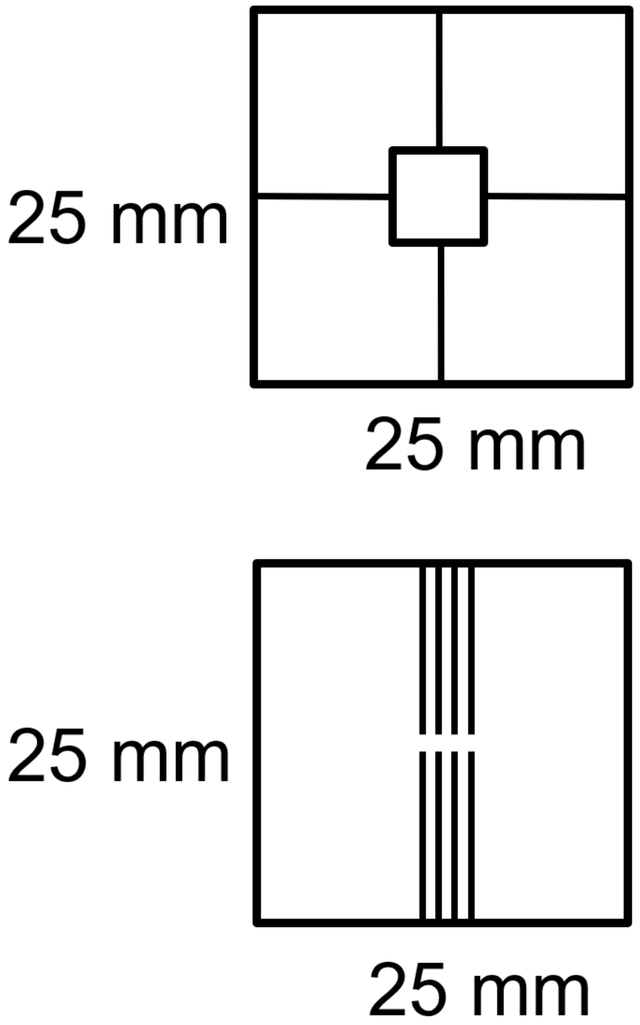
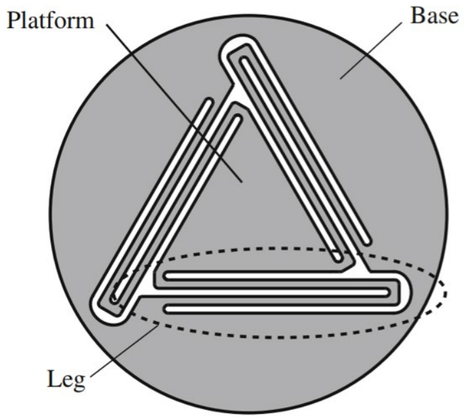
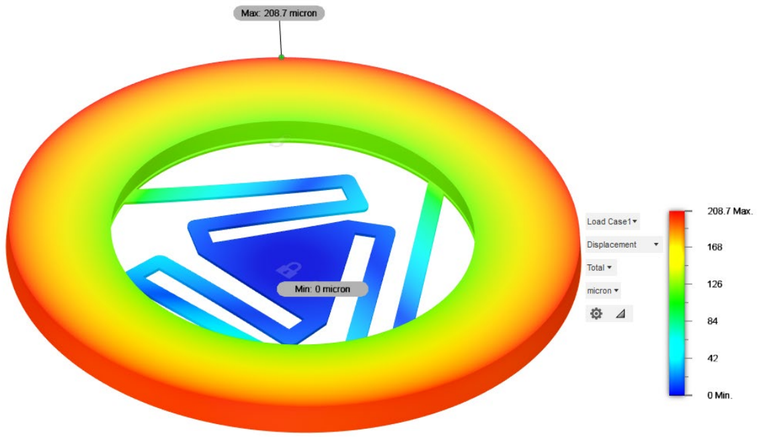




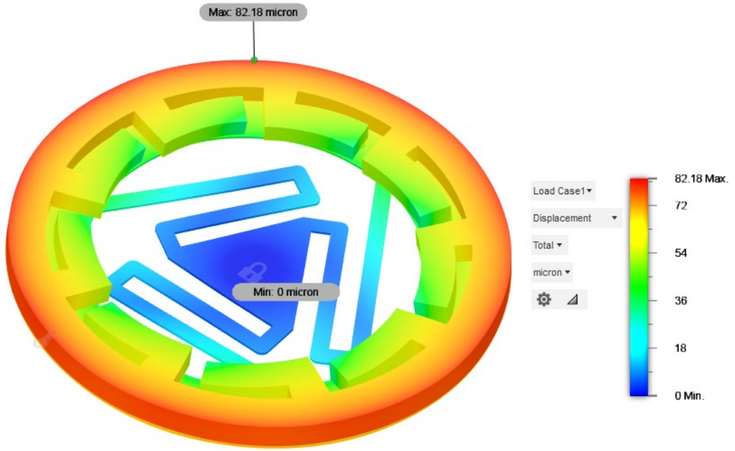
Example of a three-legged orthoplanar spring

Thermal Cooling Displacements Due to PCB/SiC CTE Differences

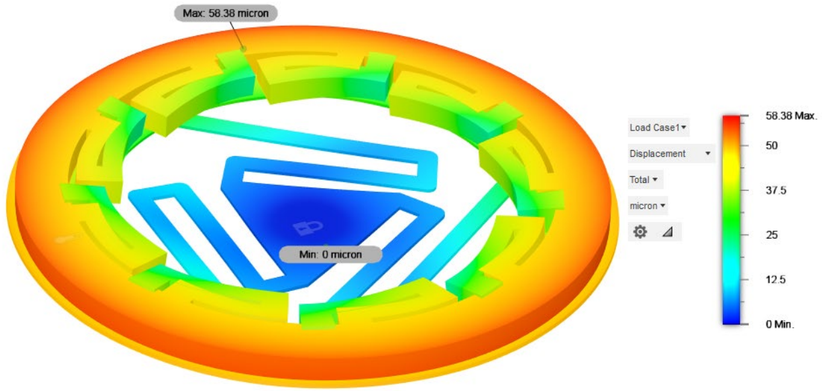
Nielson Scientific



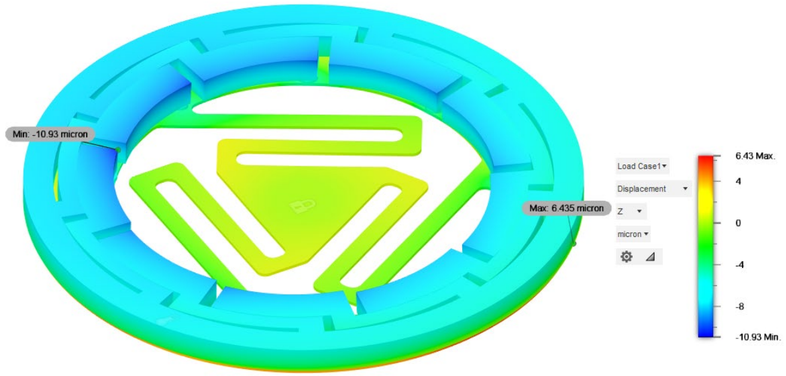
208 µm



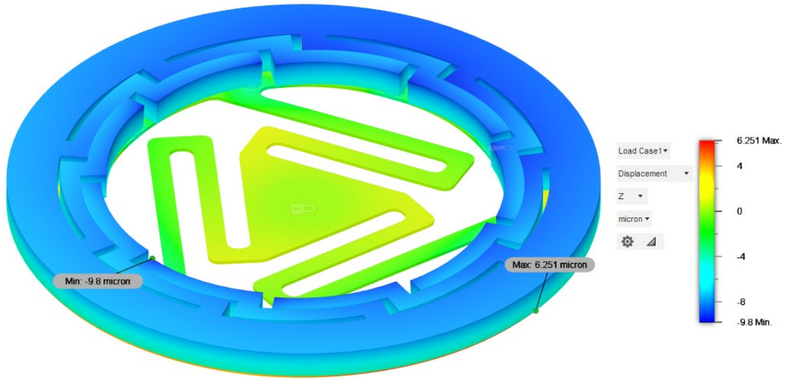
82 µm



58 µm



17 µm



16 µm

Thermal Cooling Stresses

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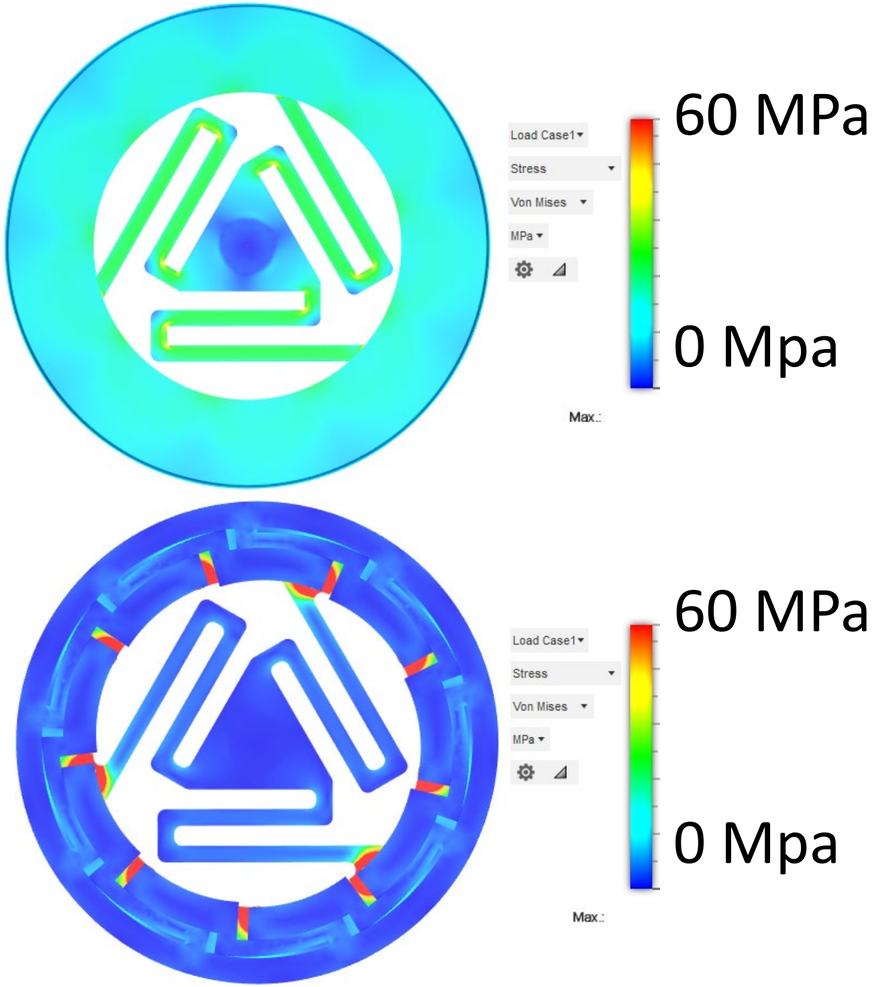
- SiC tether stress is less than 30 MPa without flexures in PCB
- SiC tether stress is less than 10 MPa with flexures in PCB
- Max stress happens in solder due to material differences



Solder Cooling Stresses

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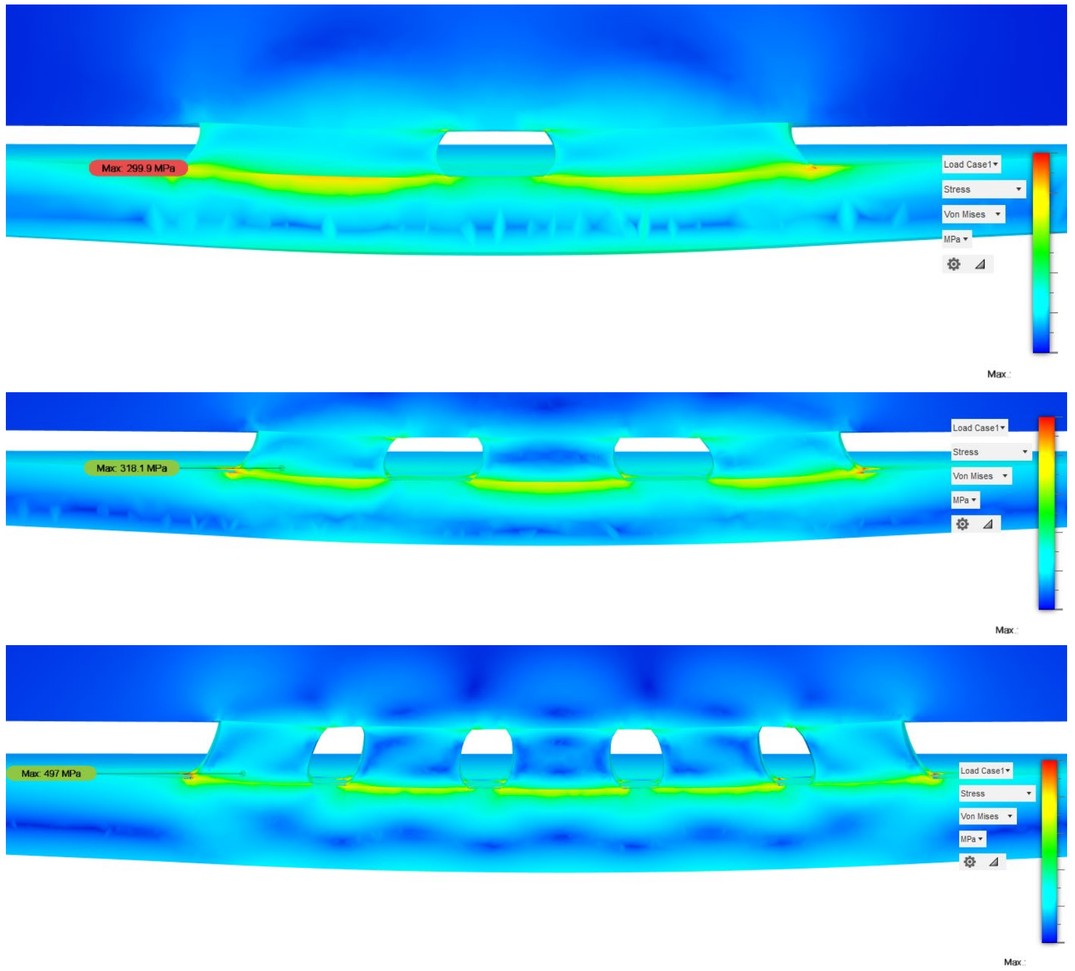
- Stress is reduced for taller, skinnier solder bumps
- Multiple small contact points improve mechanical connection robustness against thermally induced stresses



200 MPa

0 Mpa

FEA Analysis of a 50 µm Displacement

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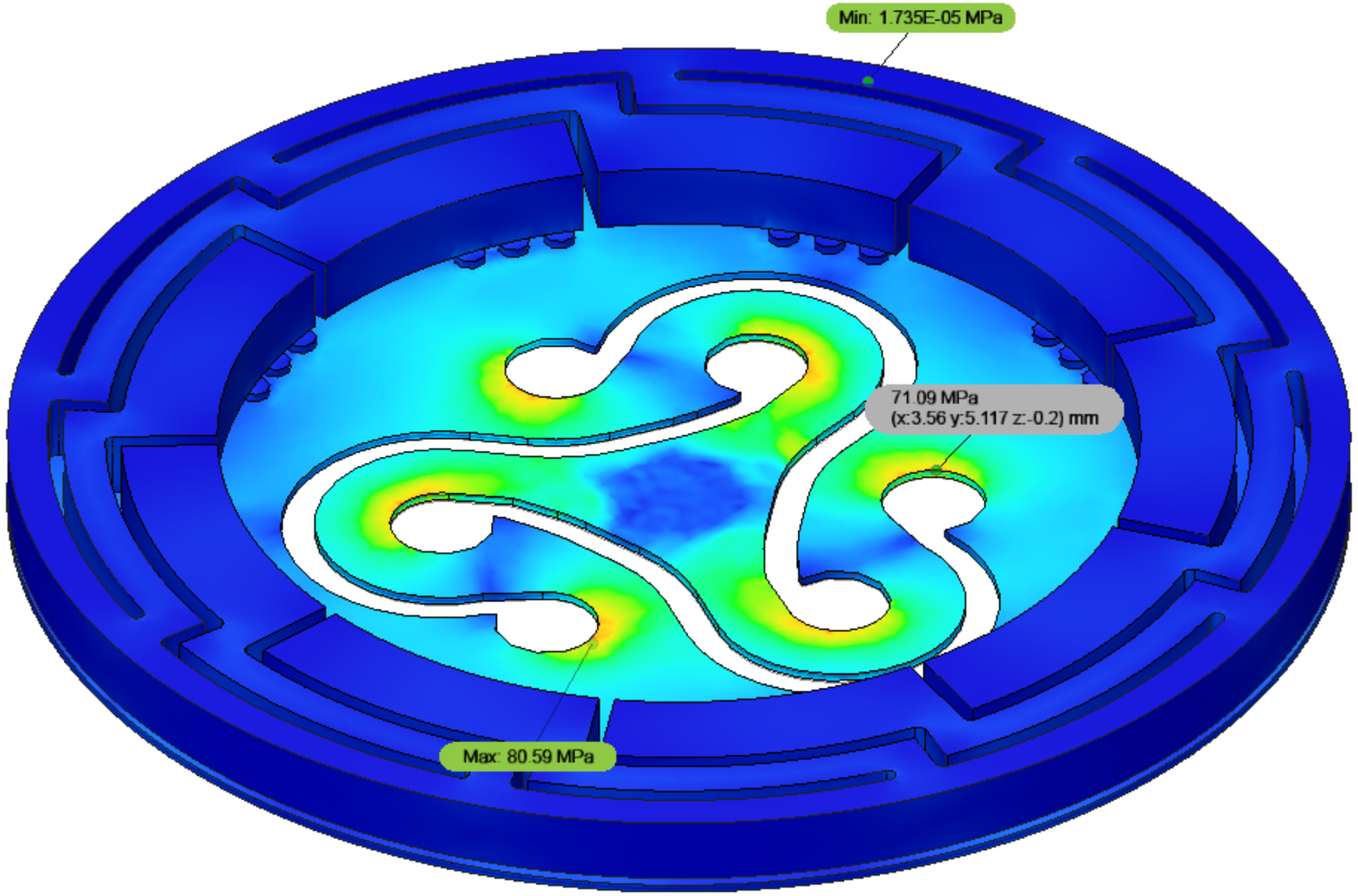

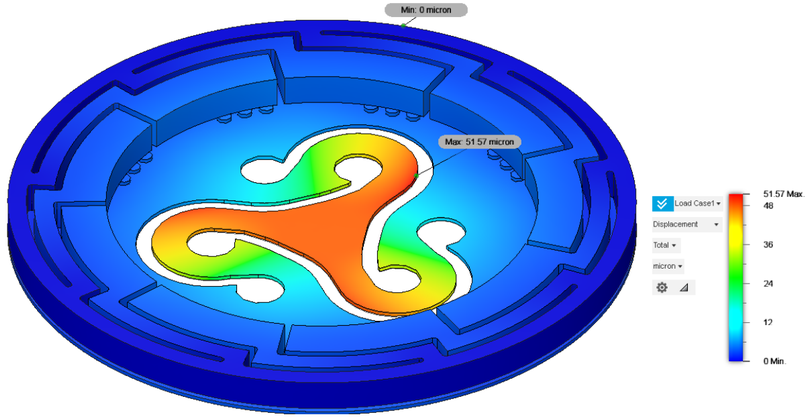

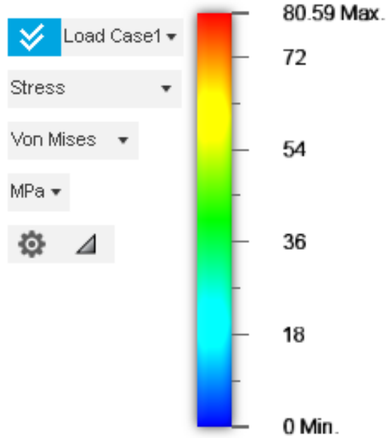

Front/Back Traces, Vias, and Probe Tips

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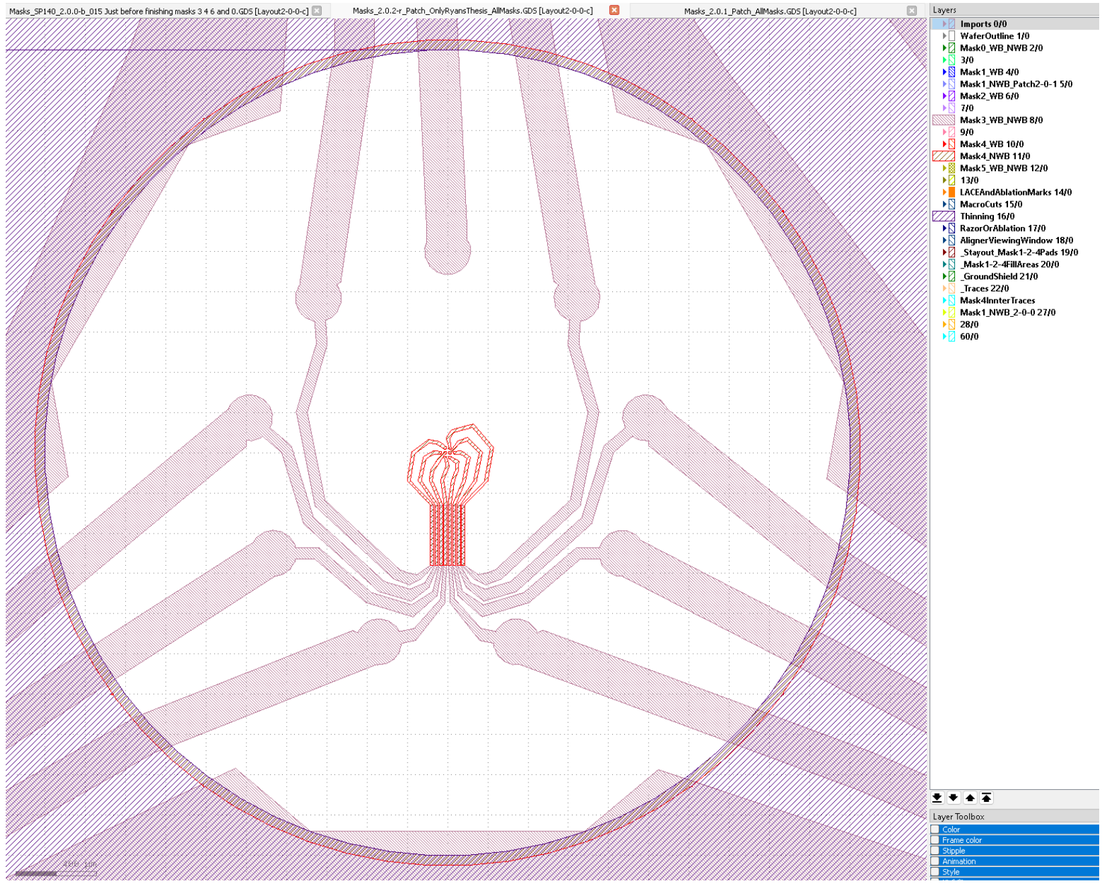

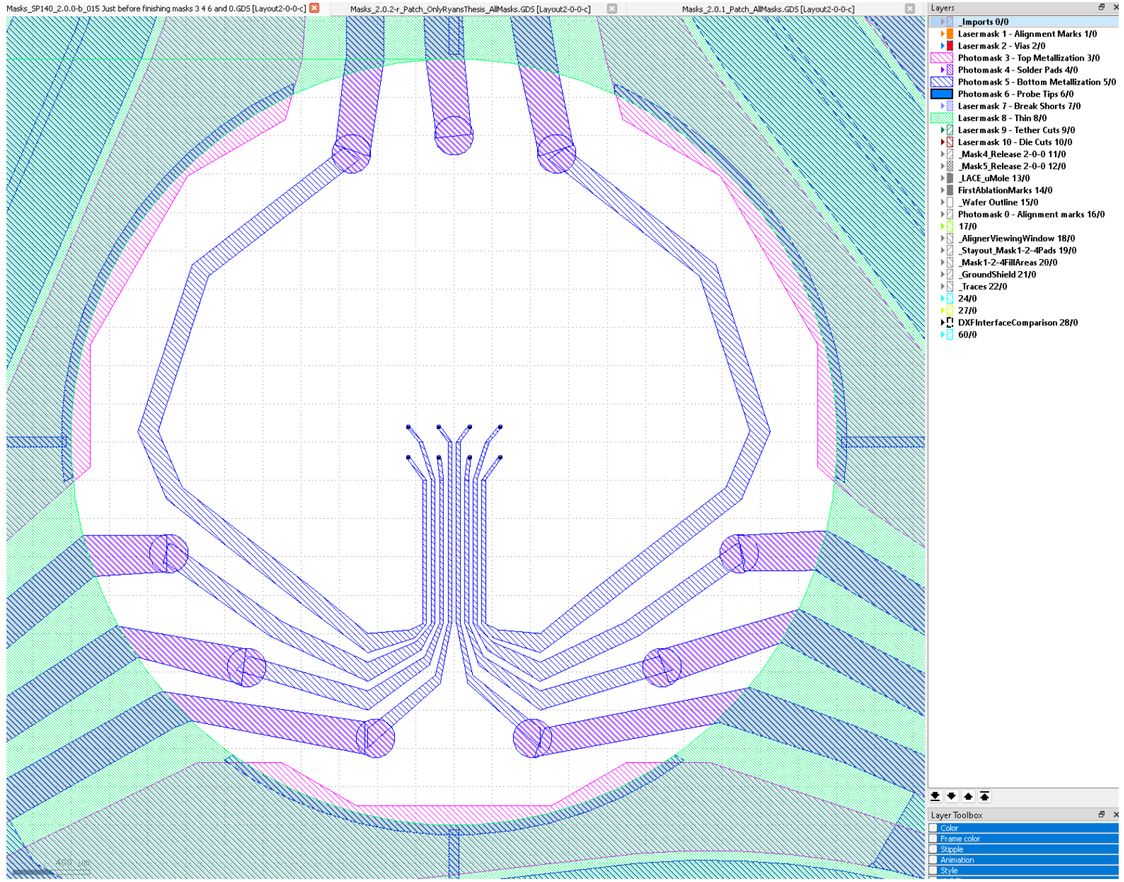

Final SiC Die

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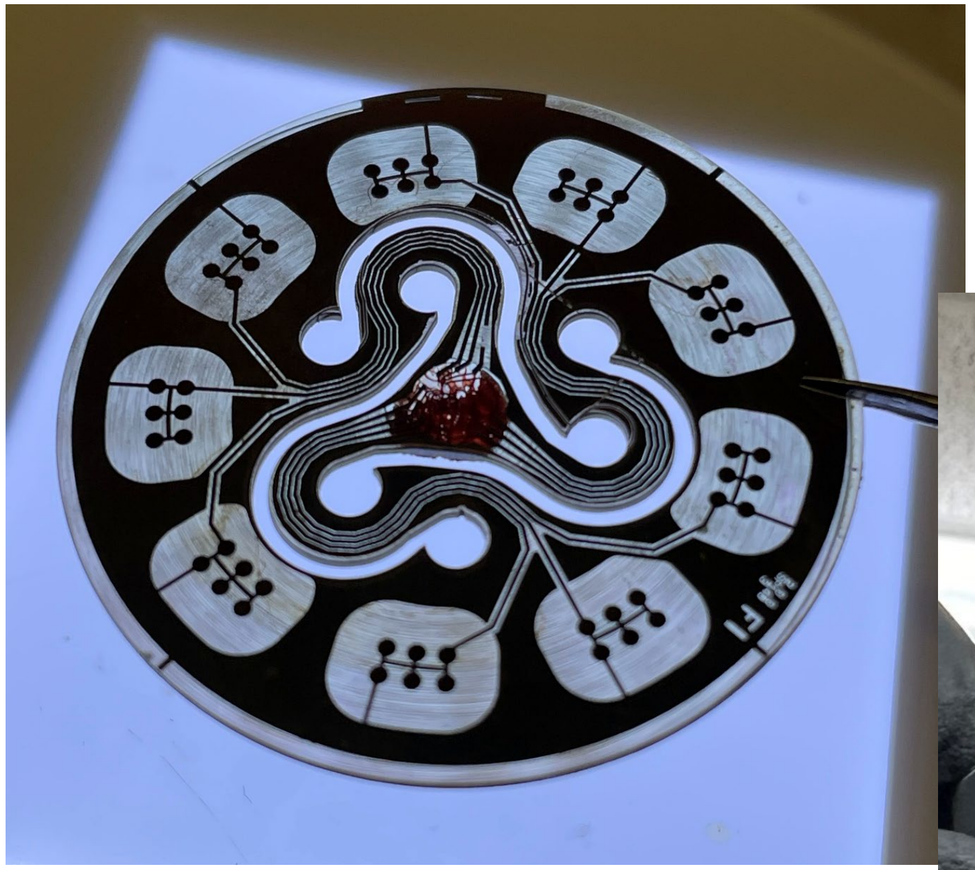
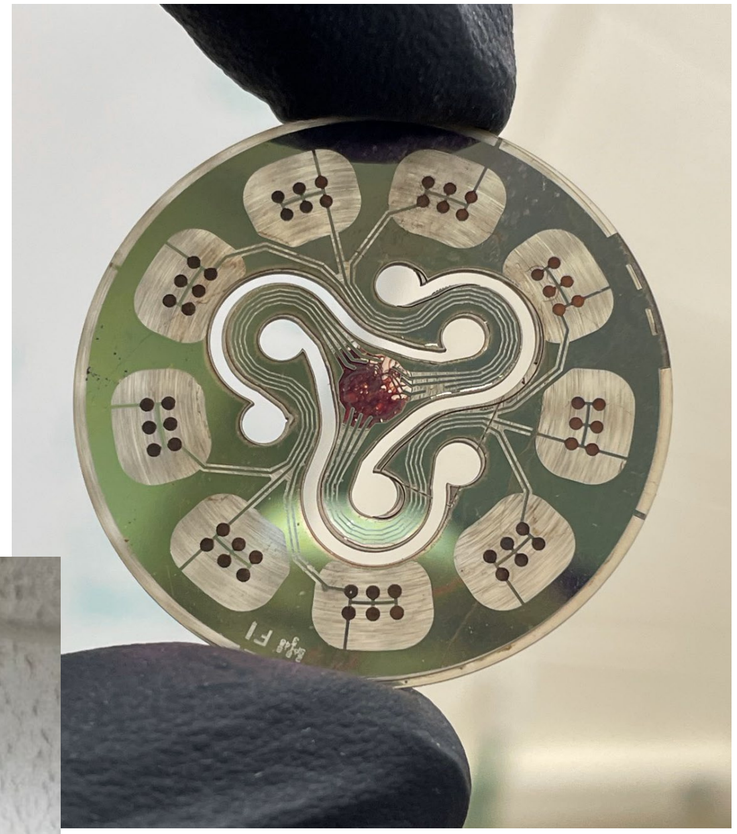




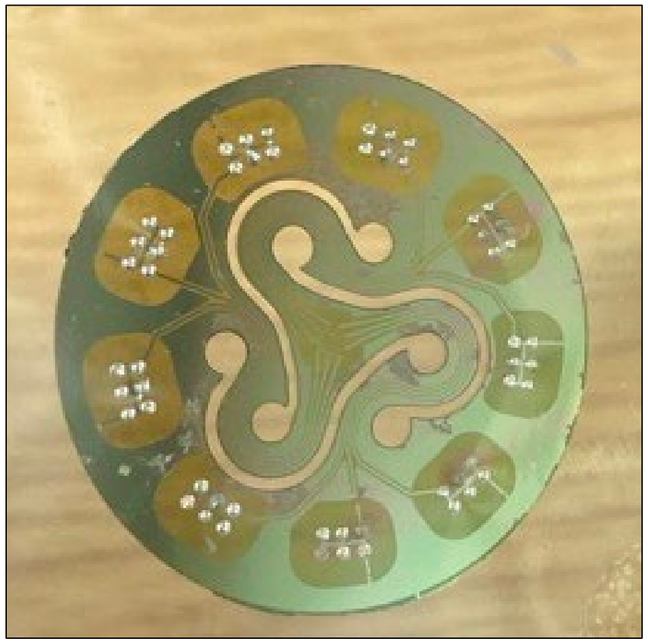
Turning a SiC Die into a Probe Card

Dalton Roehl

PCB Attachment

- The Flexure PCB is attached to the SiC die using a low temp solder to form a mechanical and electrical connection.
- The flexures within the PCB mitigate the radial mechanical stress from the cryogenic shrinkage.
- The 6-point solder positions provide a strong yet flexible connection.

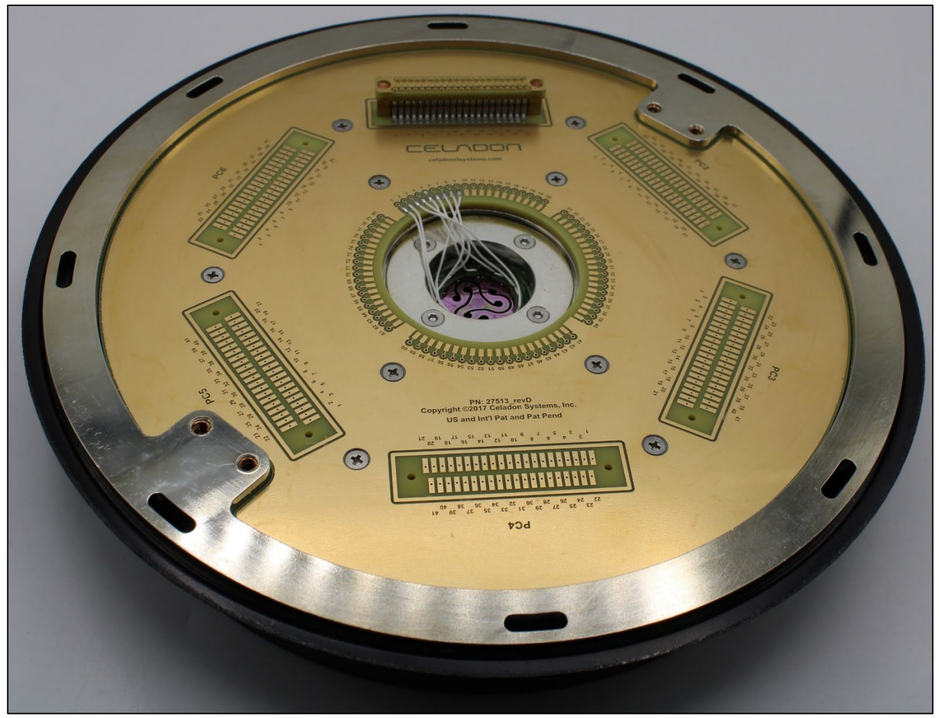
Flexure PCB

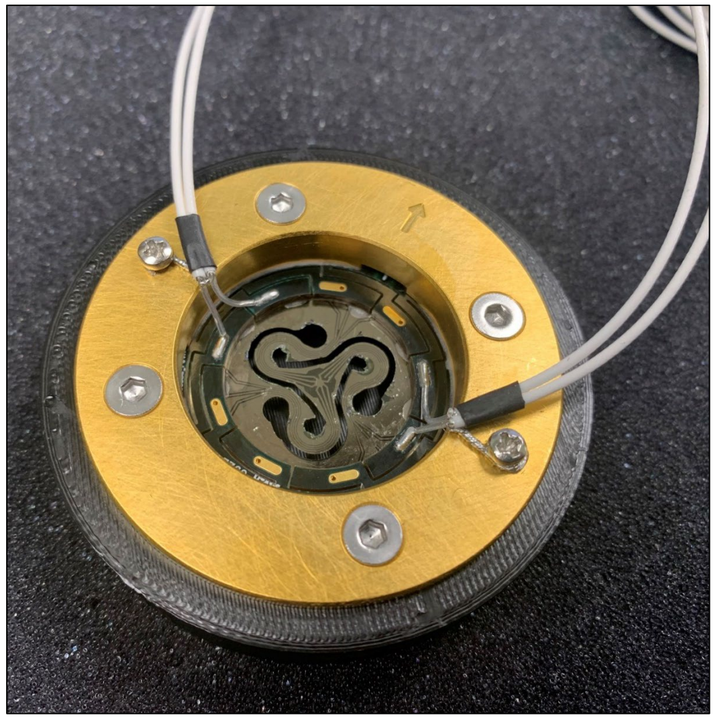


SiC Die

Final Assembly

- The finishing process for the product is to terminate the Flexure PCB to a usable interface.
- This has been done by either direct cable out, or to a larger PCB

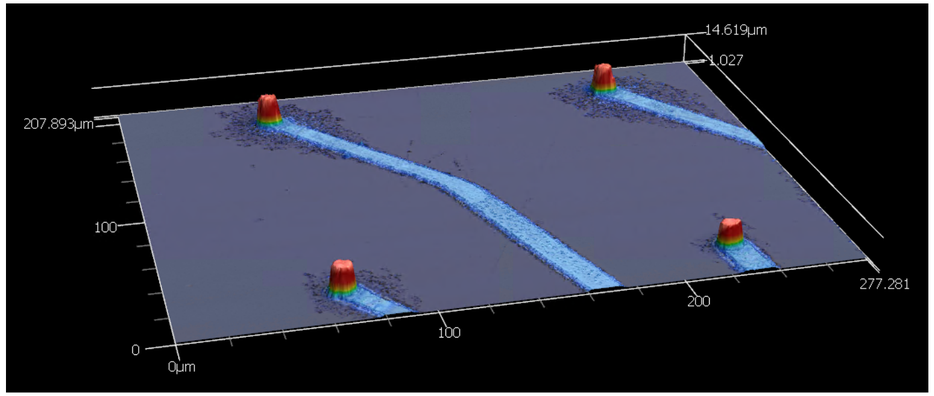


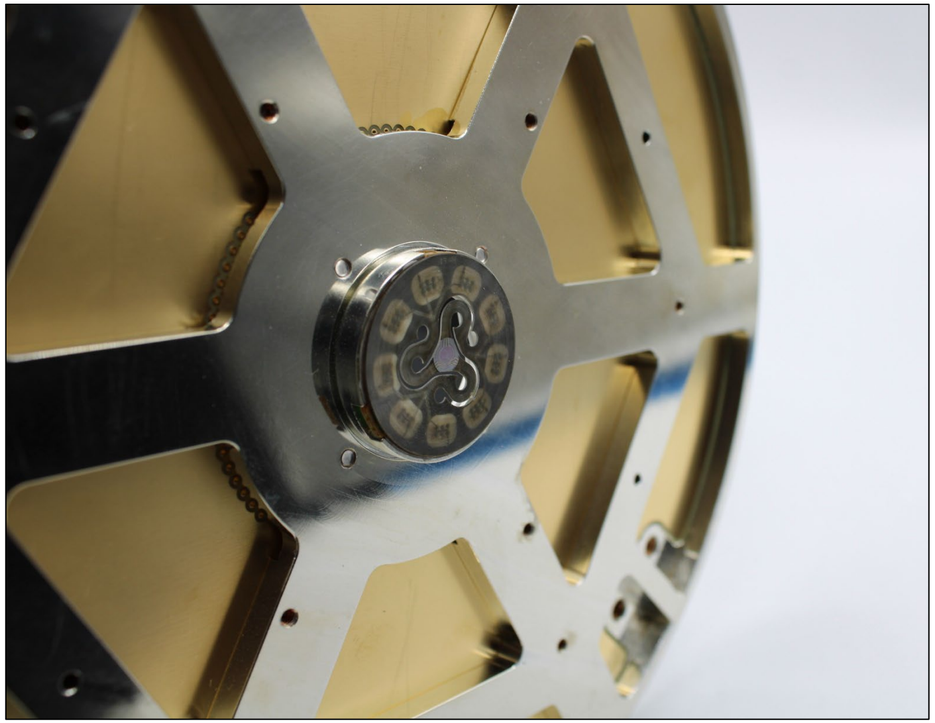


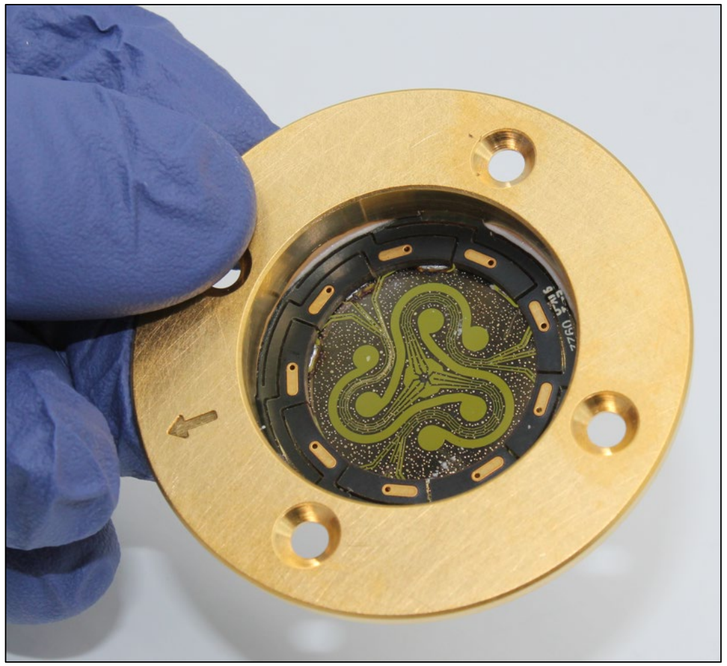
Finished Product

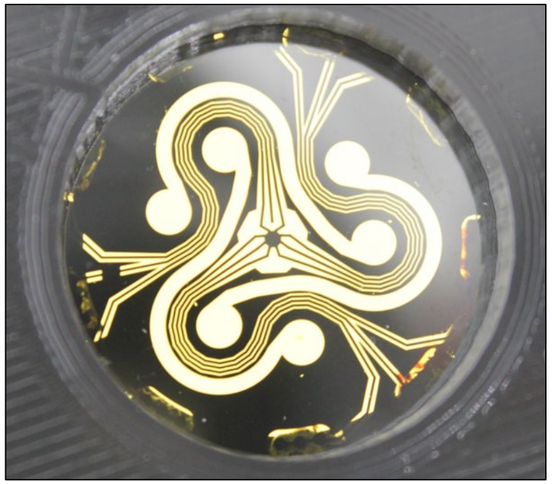
Key Features

- Cryogenic Probing expected down to 2K
- Clear Optical Path for top-down alignment “See-through”.
- MEMS style probes for pad arrays.
- Small probe tips at 8 µm diameter
- Extremely tight pitch down to 20 µm.
- Future plan for hundreds of probes.









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CUG011 Reliable Solutions for Cryogenic On-Wafer Test

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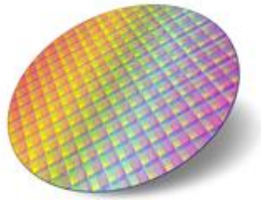
March 21, 2025

Why Cryogenic On-Wafer Test?

Cryogenic test requirement [4K, 77K common]

- Current technology and medical advancements are requiring the need for challenging cryogenic tests with higher throughput.



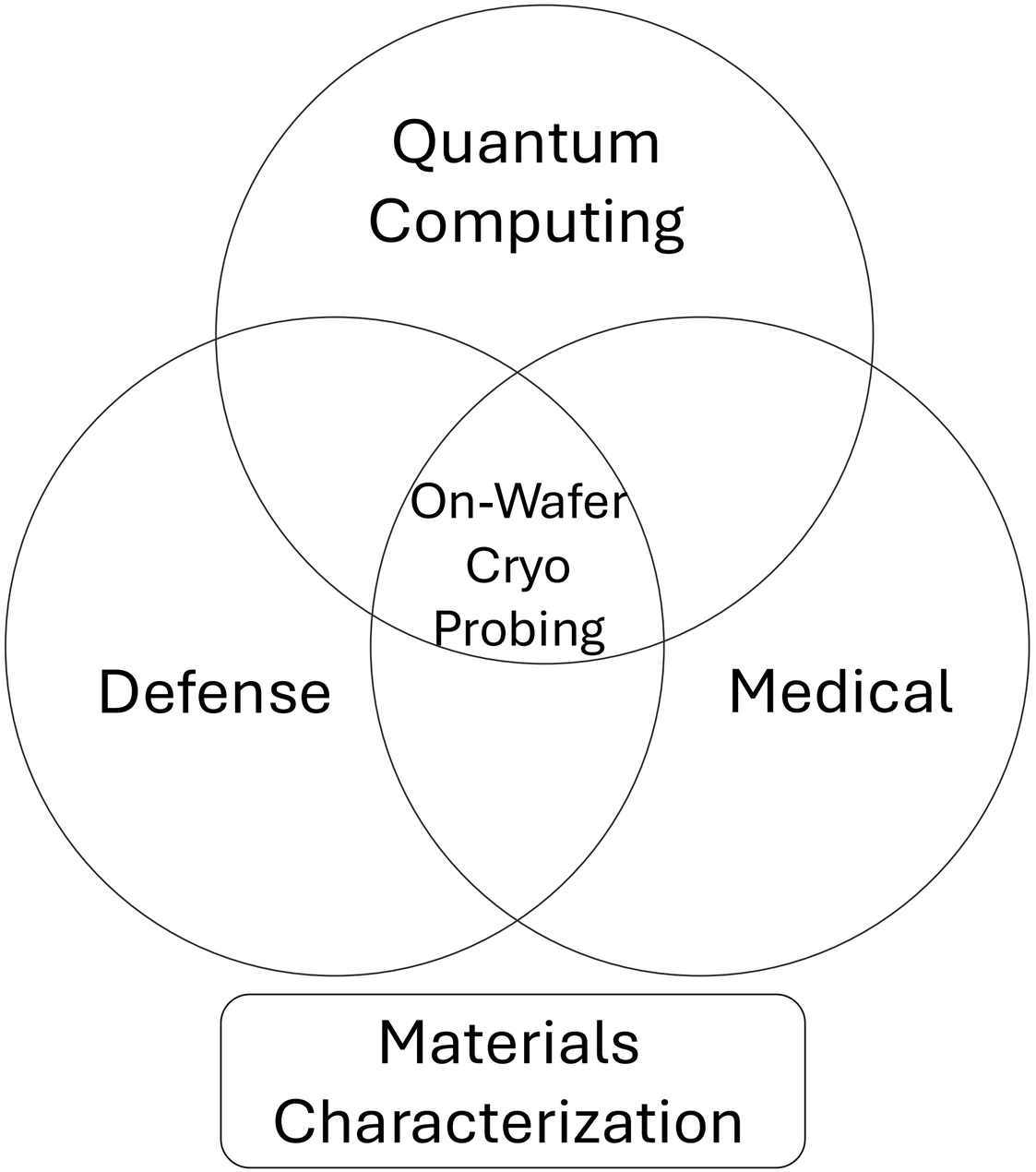
Hardware to *physically* handle DUT, Wafer, or Sample

- For optimal cryogenic test, a cryogenic **probe station** is used to **handle and thermalize** the DUT, Wafer, multiple-samples, or single die/chips.

Hardware to *electrically* test DUT, Wafer, or Sample

- To take electrical measurements, **probes and probe cards** are used to contact the DUT, Wafer, or Sample to transpose the signal into a larger environment to interface to test hardware.

Industries



Cryogenic Probe Card Types

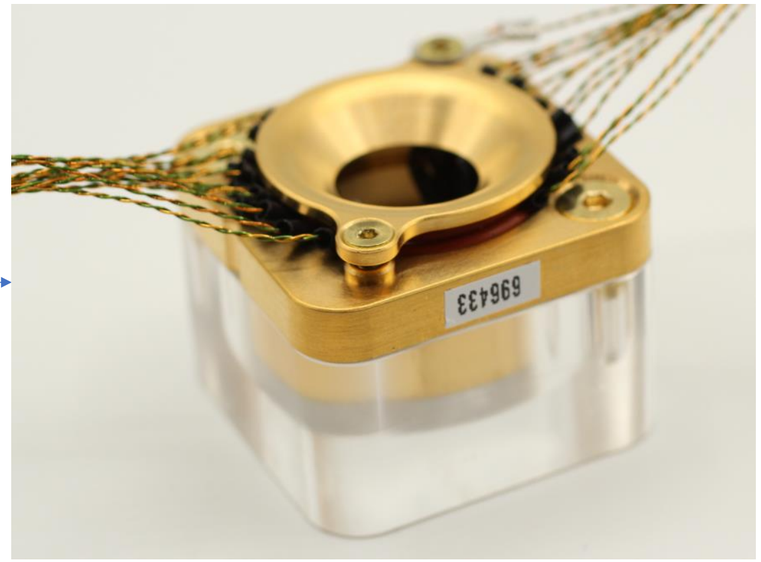
- Cryostat with micro-positioners
- Cryostat without micro-positioners
  - Lower cost, lower facility resources, lower throughput

- Cryoprober with moving chuck [wafer]
- Cryoprober with moving chuck [singulated die / waffle pack]
  - High cost, lots of facility resources needed, higher throughput

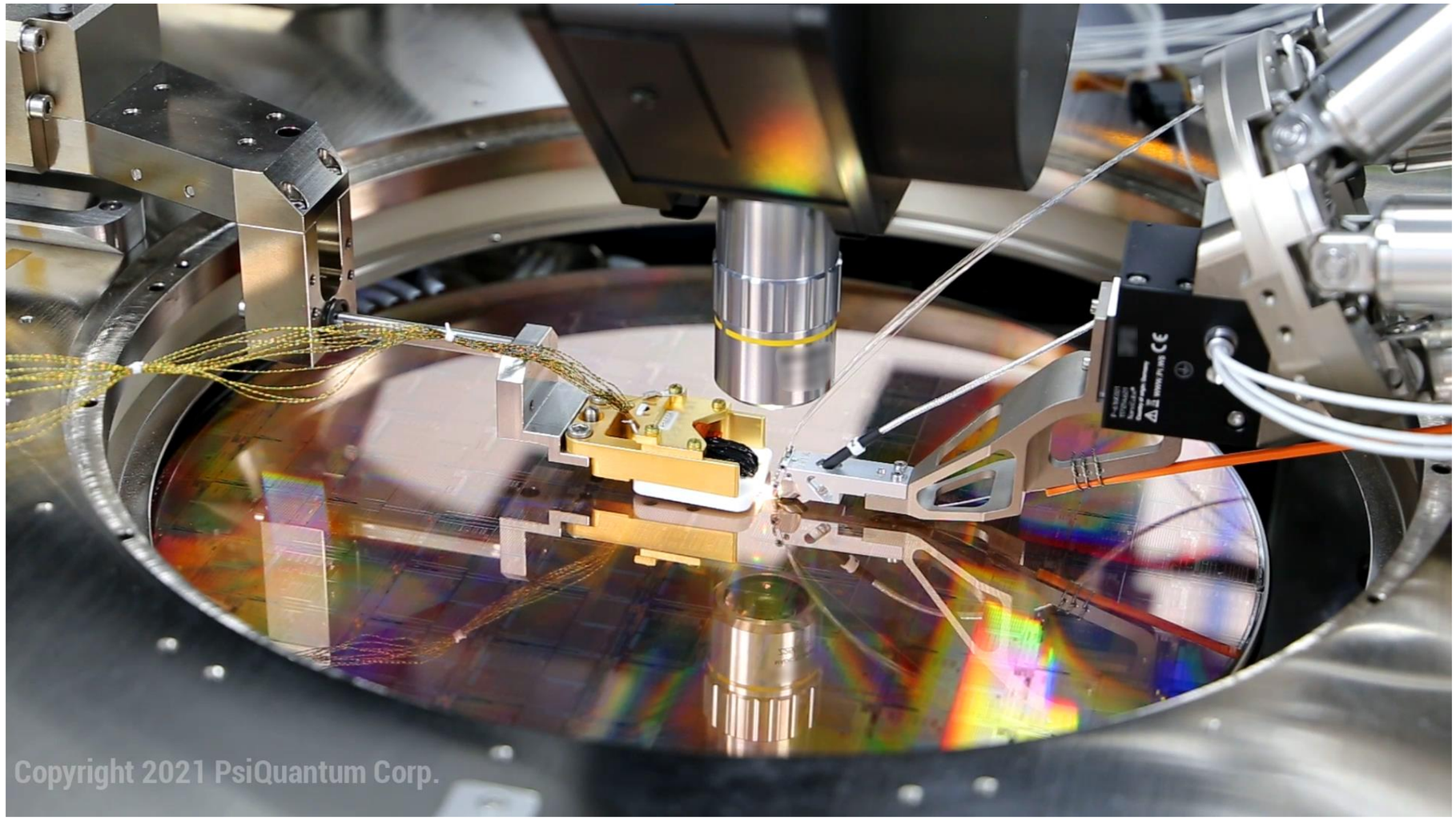
Cryostat with micro-positioners

- Similar to standard on-wafer lab probe with micropositioners, a cost-effective method to test on-wafer at cryogenic temperatures is to have a positioner arm go through the cold chamber wall.
  - This positioner would then have either a “MiniTile” or a “VersaTile” depending on the application and probe approach requirements.

- Considerations for designing probe cards for cryogenic applications:
  - Material
  - Plating
  - Wiring
  - Strain Relief



Cryo probe card in room temp SiPh Application



Forbes 2022 “PsiQuantum Has A Goal For Its Million Qubit Photonic Quantum Computer To Outperform Every Supercomputer On The Planet”

Cryostat without micro-positioners

- In some applications, due to the nature of the test, a positioner arm cannot be used
  - Need to reach lower temperatures
  - Layout not compatible with MiniTile or VersaTile

- For this, Celadon developed the “MobileProbe”

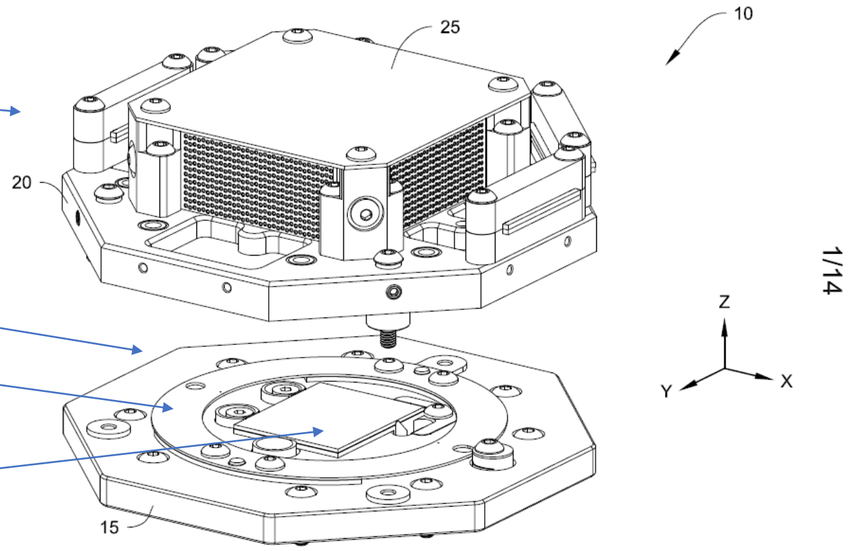
Two primary mechanical parts

- Probe Card
  Probes are on the underside
- Base

- Movable Component:
  - Flexure for Alignment Reference

- Customer chip or DUT

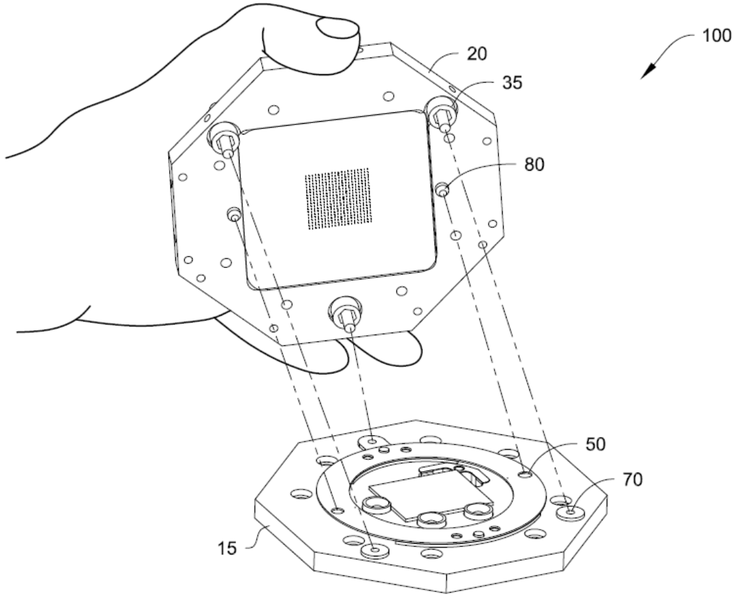
Fig. 1



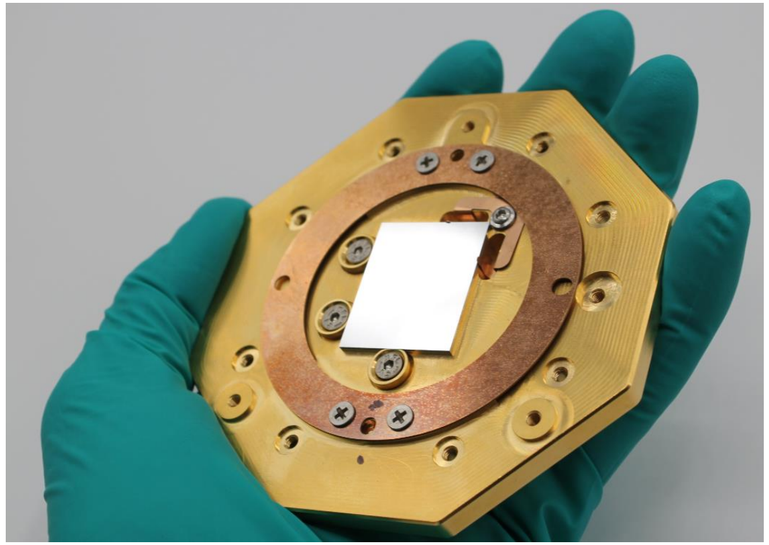
Functionality

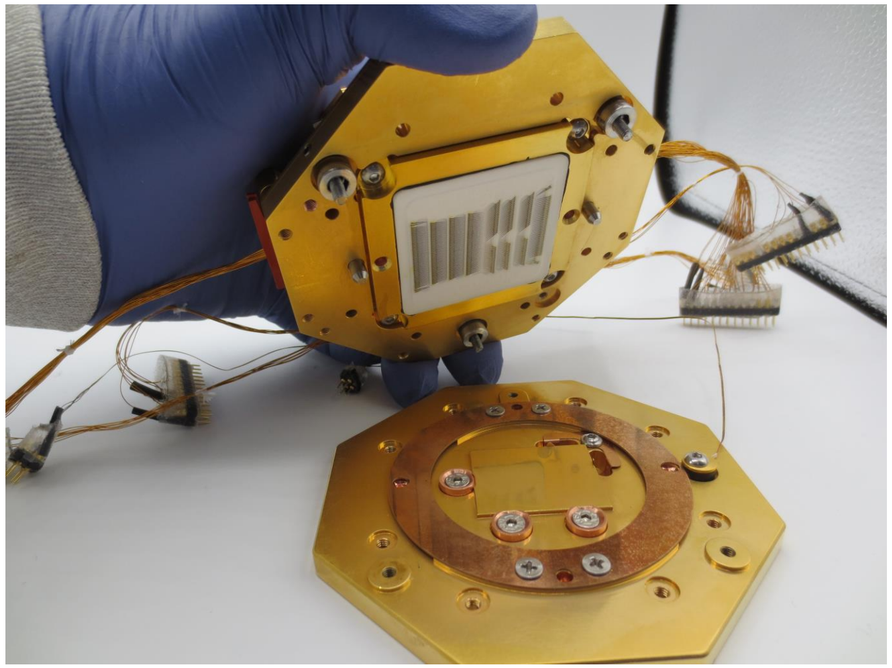
- The Celadon MobileProbe™ uses a kinematic system of holes, tapered pins, and a precise fiducial to ensure repeatable and accurate probing. The integrate bumper stops ensure the card is not crashed or overdriven to the point of probe damage.
  - Celadon has not tested long-term touchdown count.
  - Celadon can integrate TDS probes and Silicon Diode Thermal Sensor feedback in this system.
  - Celadon may modify architecture to include PCB with components.
  - Celadon may design to test multiple chips at once.

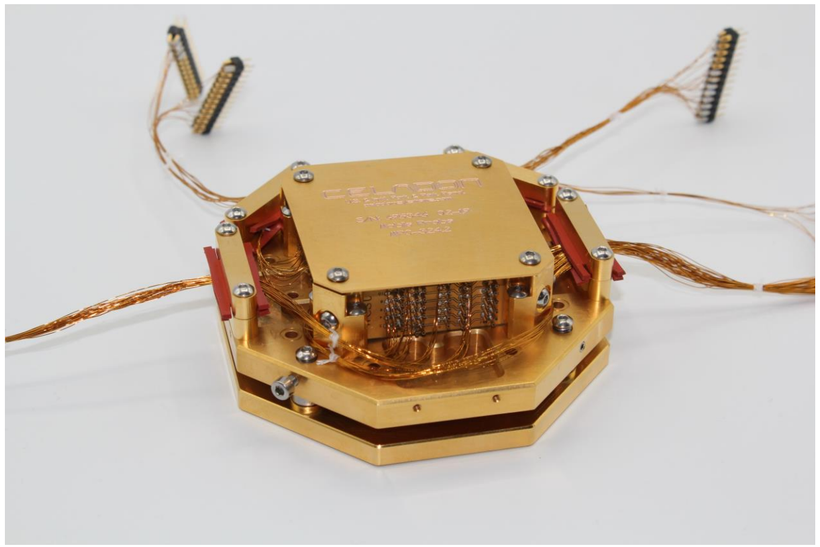
Fig. 9A



MobileProbe Images

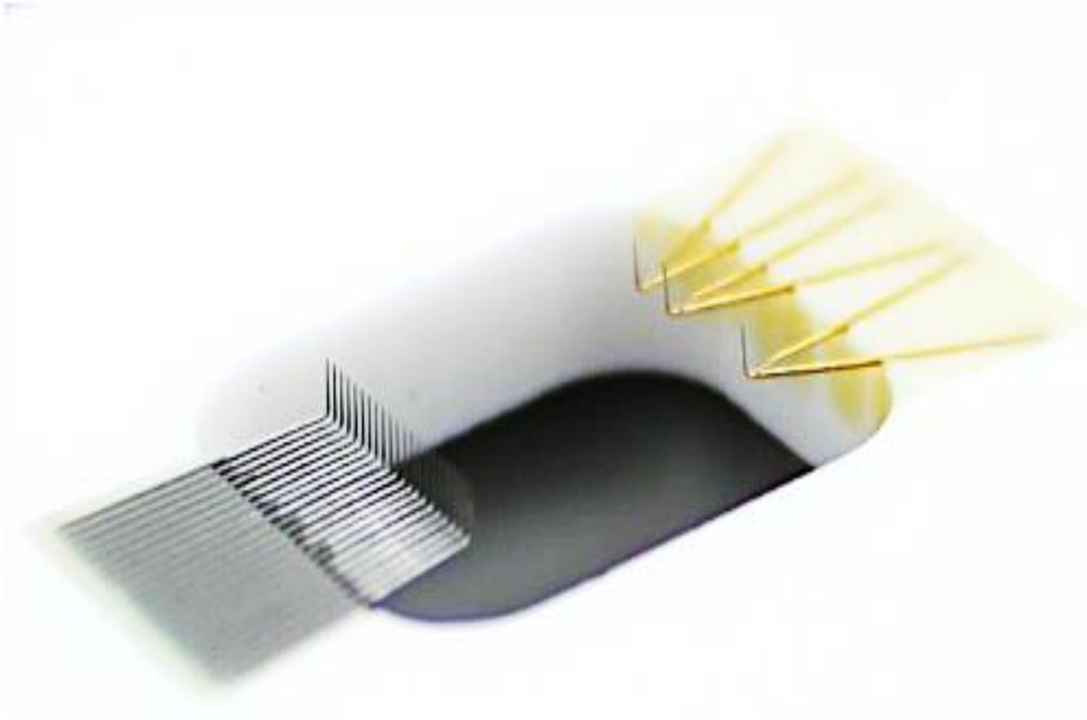






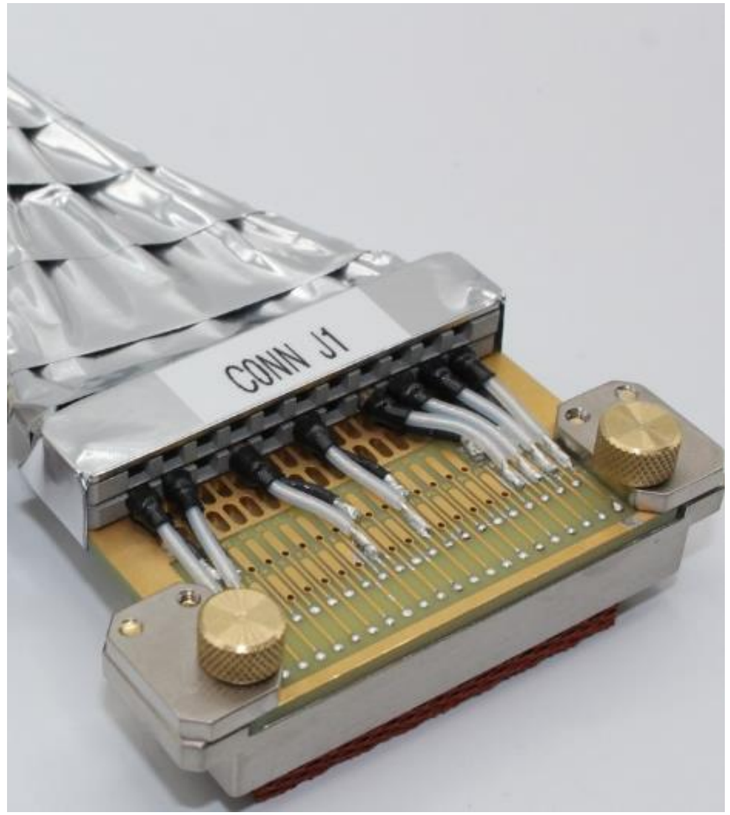
CryoProber Probe Card Solutions

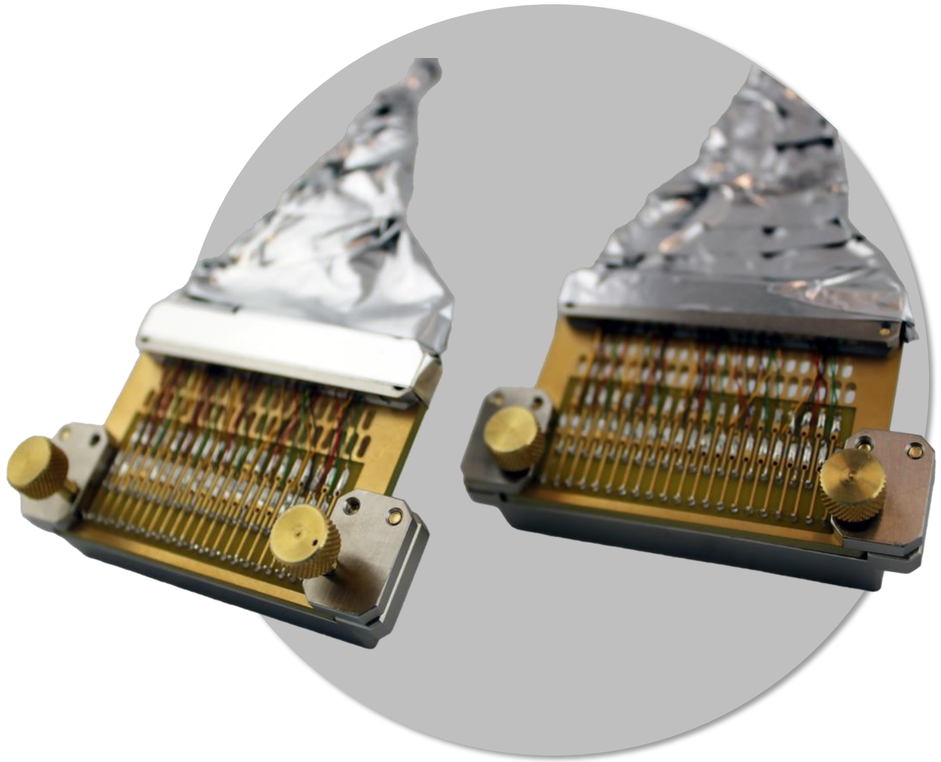
- For this level of cryo probing, the entire chamber is a vacuum; thus, you can no longer use a vacuum chuck to hold the wafer.
  - Sometimes the chips are placed in a waffle pack
  - Sometimes the chips are held down with a small clip
- The result being that the probe card “toe drop” must be significantly more than a standard Celadon card.
  - [Normal is 250µm toe length, some cryo systems need **1,250µm!**]



CONSIDERATIONS FOR TESTING AT 4K AND BELOW

- Cryogenic cables are specially selected for both thermal considerations and signal integrity. Some signals are more sensitive, requiring a larger coax wire. Less sensitive signals can go through very small hookup wires to minimize thermal mass.

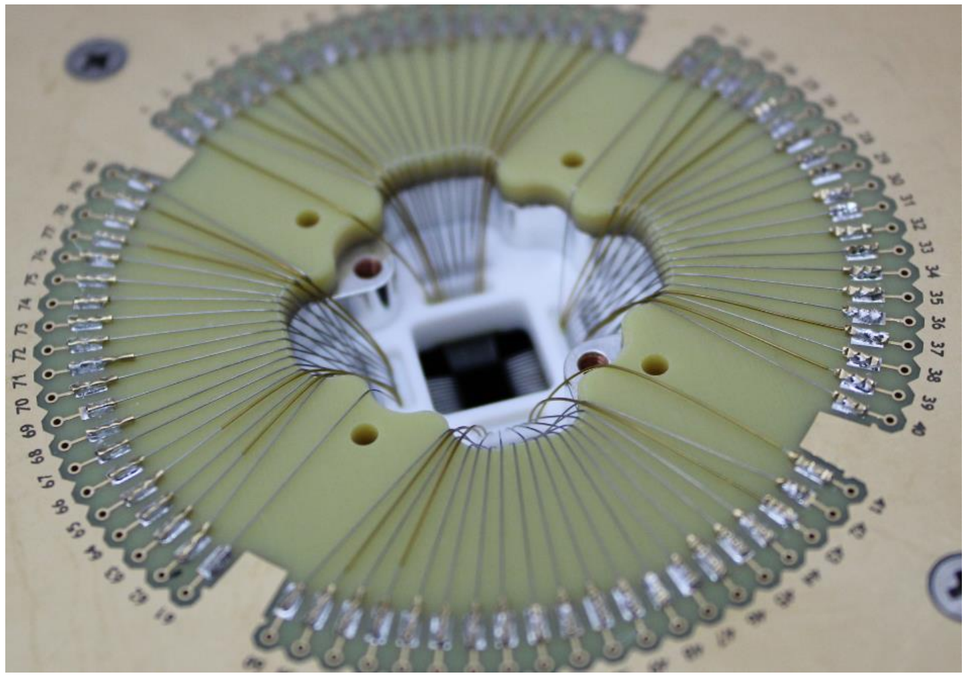




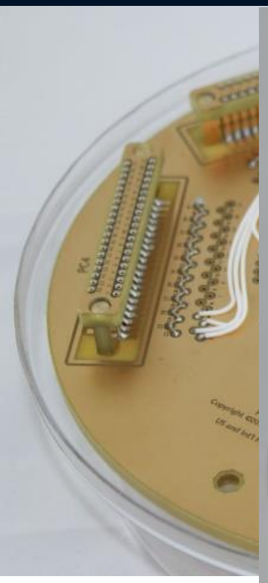
Unique Requirements Drive Unique Solutions

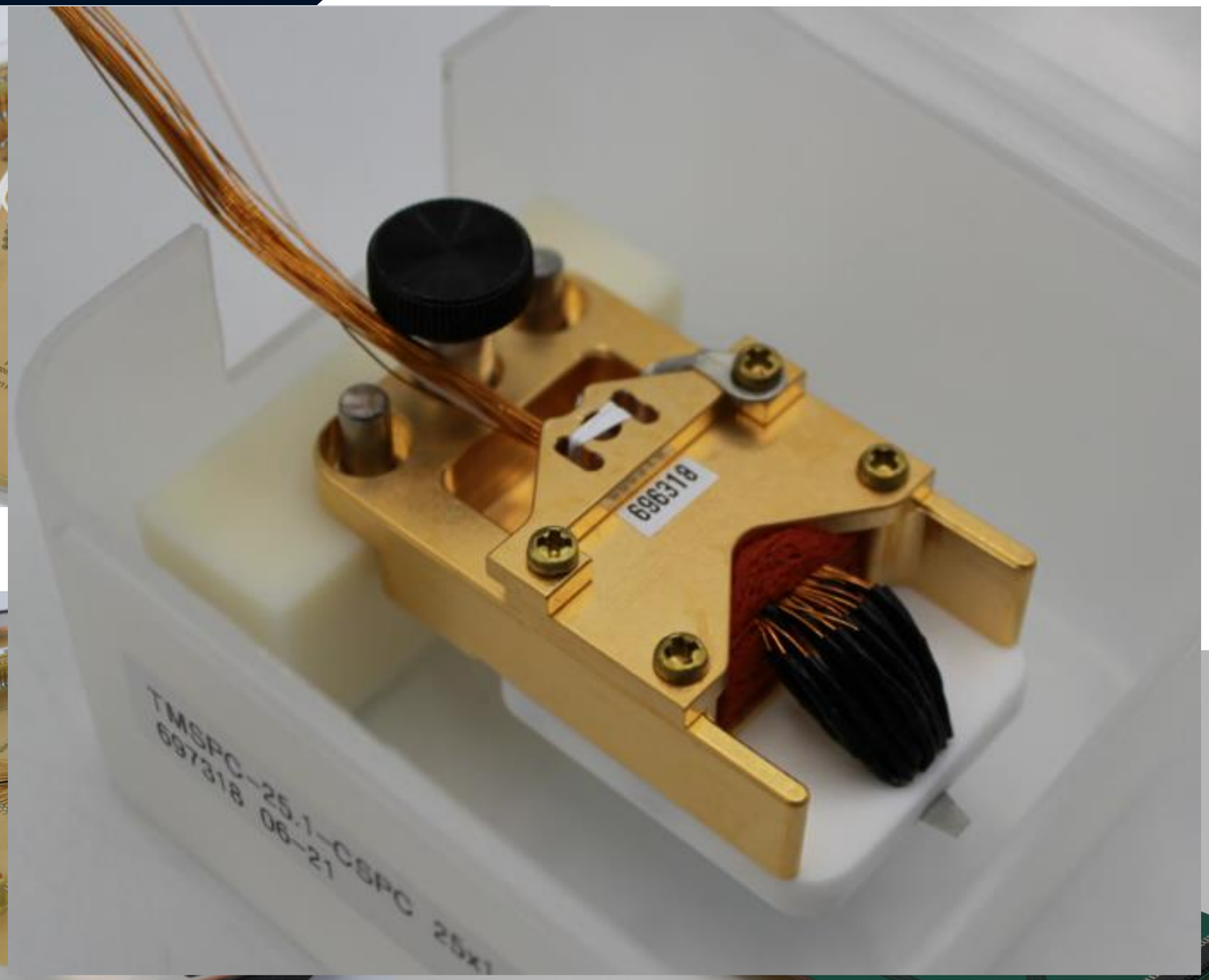
- For a totally non-ferrous solutions, Celadon had to developed a good way to solder Wre [Tungsten Rhenium] probes to a PCB. Normally this would be Nickel plated.

- Custom stiffeners [thermal mass reduction]
- Custom nonmagnetic plating processes



Many Different Styles of Cards





Acknowledgements

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